sev10

FMEDA · ISO 26262-5 hardware metrics

Corner brake ECU (EMB)

Company name	sev10
Engineering location	sev10 (remote engagement)
Customer name	Quillon Motors
Model year / program(s)	Electric pickup, brake-by-wire with blended braking (illustrative program)
Subject	Corner brake ECU, TI TIDA-020106 PCB VerB
FMEDA ID number	S10-QLN-FMEDA-001
Revision	A (draft for client review)
Start date	2026-09-28
Revision date	2026-09-28
Design responsibility	Texas Instruments (reference design TIDA-020106); integration: Quillon Motors
Cross-functional team	sev10 functional safety and hardware; Quillon Motors brake systems (review)
Prepared by	sev10
Reviewed by	Pending: sev10 internal verification; Quillon Motors
Confidentiality level	Confidential. Prepared for Quillon Motors.

Basis

Safety goals and ASILs from S10-QLN-HARA-001 Rev B. Failure chains, safety mechanisms and actions from S10-QLN-DFMEA-001 Rev A; each row names the DFMEA rows it rests on. Method: ISO 26262-5:2018 clause 8 (SPFM, LFM), clause 9 (PMHF) and Annex D (diagnostic coverage).

Scope

Rev A computes SG-01, SG-02, SG-03, SG-04, SG-05, SG-07 on provisional data. The other goals are not computed in this example package; their tabs say what the computation would cover and what it waits for. Most IC values sit in TI parts whose FMEDAs are available on request only (OQ-007). Mission profile, failure-rate sources and equations: Basis tab. Shared causes: Dependent failures tab. Latent-fault test intervals against the FTTI and the mechanism-to-requirement matrix follow in Rev B.

Scenarios

A, VerB as built: Published hardware (R58 fitted, PMIC SAFE_OUT1 unconnected, no EPB terminal readback). Software safety mechanisms the hardware allows are credited as the DFMEA specifies them (ASSUMED, OQ-032). B, With DFMEA actions: R58, Q6, R53 and C63 not fitted (EPB-401, EPB-404, EPB-406), SAFE_OUT1 pulls U7 nSLEEP low (EPB-408), 10 kOhm DRVOFF pull-up (EPB-121), OUTA/OUTB voltage readback (EPB-211, EPB-314), periodic cut-off test (EPB-411); for SG-01, U5 input pull resistors (BLD-102), SAFE_OUT1 also to U5 nSLEEP (BLD-120), motor-phase isolation driven independently of U5 (BLD-201, BLD-118), angle-input pull-downs (ANG-101), split ADC modules and a reference check (ANG-306, PMC-201); for SG-05, a WSSO pull-down at U14.31 (WSS-302); for SG-02, the corner-status timeout as a vehicle requirement (PMC-118), stay unavailable after an unplanned reset (PMC-419), a drive-response monitor (BLD-104, BLD-110, BLD-202) and per-channel CAN loss reporting (CAN-105); for SG-07, soft-termination AEC-Q200 bus capacitors away from the board edge (SUP-417, BCK-103, BCK-104, BLD-401, EPB-201, PCB-201), 50 V 125 C parts on the 12 V rail (BCK-403, BCK-409), an IMON supply-current check (PCB-202, SUP-314) and CAF-resistant laminate with wider 48 V spacing (PCB-302, PCB-303).

Method notes

One row per component failure mode. Class: Safe (no effect on the goal), Direct (violates the goal on its own: single-point or residual), Latent (violates it only together with a second fault, by disabling a mechanism active in that scenario), n/a (not counted for this goal or not present in the scenario). λ part comes from the FIT data tab and DC from the Safety mechanisms tab, so each value is set once. Each latent row names its partner rows; their λ enters the dual-point PMHF term. Equations: Basis tab.

Marking

Orange cells mark values that rest on an assumption. Each has a comment with the reason code, the basis and the question that would close it, and the row lists them in its ASSUMED column. All are listed on the Assumptions tab, grouped by what closes them; the Summary counts them and shows which ones the result depends on.

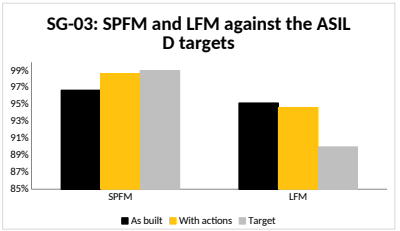
Corner brake ECU (EMB) · hardware metrics by safety goal

TIDA-020106 PCB VerB for Quillon Motors. Goals from S10-QLN-HARA-001 Rev B. ISO 26262-5 SPFM, LFM and PMHF, computed live from the goal tabs. Provisional: every IC value rests on TI data not yet received.

SG-03, avoid parking-brake application while the vehicle is moving, unless the driver requests it (ASIL D)

	SPFM · target ≥ 99%	LFM · target ≥ 90%	PMHF (FIT) · item < 10 FIT; corner share open (OQ-046)
As built	**96.70%**	**95.19%**	**3.99**
With actions	**98.65%**	**94.65%**	**1.63**

Black = below target, yellow = meets it. PMHF is shown against the item-level value only; it is not judged until Quillon Motors allocates the corner ECU's share (OQ-046).



Assumption status

Assumed values	Close with TI data	Close with the firmware specification	Close with client data	Set by sev10 judgment
393	**280**	**36**	**44**	**33**

Every assumed value is marked orange in the workbook with its reason and the question that closes it, and listed on the Assumptions tab. The sensitivity table below shows which of them the result depends on.

What drives the result

1. As built, SG-03 misses its SPFM target (96.7% against 99%). Three faults have no working mechanism: a U7 output stage that drives the apply direction on its own (the Q11 cut-off cannot open because R58 ties its gate to the bus), U14 EPB pins stuck in the drive state (the lockstep does not see them and the only reaction runs through those pins), and U7 input faults whose reaction acts in the same die.

2. The DFMEA actions reach 98.65%, just short of the target. R58, Q6, R53 and C63 not fitted, an OUTA/OUTB readback that opens the cut-off, SAFE_OUT1 to U7 nSLEEP and a periodic cut-off test (EPB-401, EPB-404, EPB-211, EPB-408, EPB-411) remove every single-point fault. The remaining 0.42 FIT over budget is supply overvoltage on the MCU rails, credited at Medium until the PMIC monitor data is known.

3. What remains is for TI and Quillon Motors to confirm. The largest residuals are then the MCU command path (TI's lockstep coverage), the supply monitors (PMIC NVM thresholds, OQ-002) and the cut-off credits, which stop an apply without releasing it (OQ-047). The TI table turns each IC assumption into the coverage its FMEDA must show; the sensitivity table shows which changes pass or fail the target.

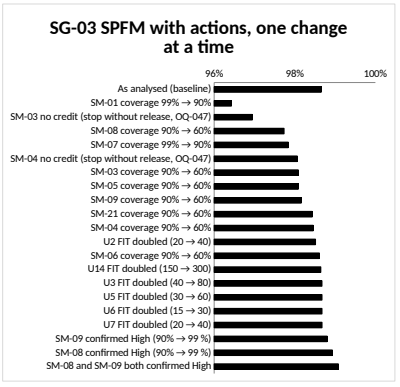
All safety goals

Goal	Title	ASIL	Status	SPFM as built	SPFM with actions	LFM as built	LFM with actions	PMHF as built (FIT)	PMHF with actions (FIT)	SPFM target	LFM target
SG-01	Avoid braking at a wheel that was not requested (unintended, excessive, misdirected or unreleased clamp force)	D	Computed (Rev A, provisional)	**87.5%**	**97.4%**	97.1%	96.8%	41.38	9.90	99%	90%
SG-02	Avoid loss of, insufficient or late braking at a wheel when braking is requested	C	Computed (Rev A, provisional)	**80.8%**	**90.4%**	99.0%	99.2%	59.40	31.19	97%	80%
SG-03	Avoid parking-brake application while the vehicle is moving, unless the driver requests it	D	Computed (Rev A, provisional)	**96.7%**	**98.7%**	95.2%	94.7%	3.99	1.63	99%	90%
SG-04	Avoid loss of parking or standstill hold while the vehicle is stationary	C	Computed (Rev A, provisional)	**94.0%**	**95.6%**	94.9%	94.4%	6.17	4.63	97%	80%
SG-05	Avoid erroneous wheel-speed information being used by the braking and stability functions	B	Computed (Rev A, provisional)	92.8%	92.8%	97.8%	97.5%	4.45	4.44	90% (recommended)	60% (recommended)
SG-06	Provide parking-brake deceleration when the driver requests it and service braking is unavailable	A	No metric targets (ASIL A)	—	—	—	—	—	—	—	—
SG-07	Avoid a thermal event (smoke, fire) of the corner ECU	B	Computed (Rev A, provisional)	**60.3%**	**76.0%**	87.2%	87.2%	28.45	13.86	90% (recommended)	60% (recommended)

ASIL B targets are the values ISO 26262-5 recommends; ASIL C and D targets are required. Goals not computed in this example say on their tab what the computation would cover.

Sensitivity of SG-03 with the DFMEA actions: one change at a time

Change	Changed to	SPFM	LFM	PMHF (FIT)	SPFM change	Meets SPFM target
As analysed (baseline)		**98.65%**	**94.65%**	**1.63**		
SM-01 coverage 99% → 90%	90%	**96.43%**	94.53%	4.33	-2.23%	no
SM-03 no credit (stop without release, OQ-047)	0%	**96.95%**	94.56%	3.70	-1.71%	no
SM-08 coverage 90% → 60%	60%	**97.73%**	94.60%	2.75	-0.92%	no
SM-07 coverage 99% → 90%	90%	**97.84%**	94.61%	2.62	-0.82%	no
SM-04 no credit (stop without release, OQ-047)	0%	**98.06%**	94.62%	2.35	-0.59%	no
SM-03 coverage 90% → 60%	60%	**98.09%**	94.62%	2.32	-0.57%	no
SM-05 coverage 90% → 60%	60%	**98.09%**	94.62%	2.32	-0.57%	no
SM-09 coverage 90% → 60%	60%	**98.16%**	94.63%	2.23	-0.50%	no
SM-21 coverage 90% → 60%	60%	**98.43%**	94.64%	1.90	-0.22%	no
SM-04 coverage 90% → 60%	60%	**98.46%**	94.64%	1.87	-0.20%	no
U2 FIT doubled (20 → 40)	40 FIT	**98.51%**	94.73%	1.83	-0.14%	no
SM-06 coverage 90% → 60%	60%	**98.61%**	94.65%	1.68	-0.04%	no
U14 FIT doubled (150 → 300)	300 FIT	**98.65%**	95.42%	2.23	-0.01%	no
U3 FIT doubled (40 → 80)	80 FIT	**98.67%**	94.66%	1.75	+0.02%	no
U5 FIT doubled (30 → 60)	60 FIT	**98.67%**	94.66%	1.63	+0.02%	no
U6 FIT doubled (15 → 30)	30 FIT	**98.68%**	94.97%	1.71	+0.02%	no
U7 FIT doubled (20 → 40)	40 FIT	**98.68%**	94.06%	1.87	+0.02%	no
SM-09 confirmed High (90% → 99 %)	99%	**98.80%**	94.66%	1.45	+0.15%	no
SM-08 confirmed High (90% → 99 %)	99%	**98.93%**	94.67%	1.30	+0.28%	no

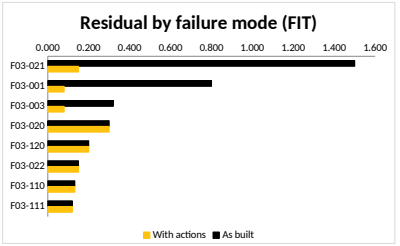


SM-08 and SM-09 both confirmed High	99%	99.08%	94.68%	1.12	+0.42%	yes
LM-13 coverage 60% → 0%	0%	**98.65%**	92.11%	1.63	0.00%	**no**
LM-04 coverage 90% → 60%	60%	**98.65%**	92.77%	1.63	0.00%	**no**
LM-05 coverage 90% → 60%	60%	**98.65%**	93.24%	1.63	0.00%	**no**
LM-03 coverage 90% → 60%	60%	**98.65%**	93.38%	1.63	0.00%	**no**
LM-02 coverage 90% → 60%	60%	**98.65%**	93.53%	1.63	0.00%	**no**
LM-06 coverage 90% → 60%	60%	**98.65%**	93.92%	1.63	0.00%	**no**
LM-07 coverage 60% → 0%	0%	**98.65%**	94.00%	1.63	0.00%	**no**
LM-08 coverage 90% → 60%	60%	**98.65%**	94.28%	1.63	0.00%	**no**
LM-01 coverage 90% → 60%	60%	**98.65%**	94.31%	1.63	0.00%	**no**

Coverage cases drop the credited value to the next Annex D band (High 99 %, Medium 90 %, Low 60 %, none) or raise it to High where TI may confirm it; FIT cases double an assumed IC failure rate, which also raises λ counted. Cases that move only the LFM (latent-fault tests) are listed last and not charted. PMHF in the FIT cases omits the small change in the dual-point term. Live formulas over the goal tab.

Largest residual contributors to SG-03 (λ SPF + λ RF, FIT)

Row	Failure mode	Element	As built	With actions
F03-021	EPB control pins (U14.2 DRVOFF, U14.11, U14.98) stuck in the drive state (port fault the lockstep does not	U14	1.500	0.150
F03-001	Output stage drives the motor in the apply direction without a command (diagonal FET pair shorted or gate	U7	0.800	0.080
F03-003	Input logic fault (EN/IN1 or PH/IN2 buffer, state machine) drives the bridge without a command	U7	0.320	0.080
F03-020	CPU, memory or bus fault produces an erroneous EPB apply command	U14	0.300	0.300
F03-120	High-side FET short: 12 V rail pulled toward 48V/12V_P	U2	0.200	0.200
F03-022	SPI-D peripheral fault writes wrong data to U7	U14	0.150	0.150
F03-110	1.25 V core regulated high (half of TI's 'output out of specification' mode)	U4	0.132	0.132
F03-111	High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	U4	0.120	0.120



What TI must confirm for SG-03 (with the DFMEA actions)

IC	Part	λ counted (FIT)	λ direct (FIT)	DC assumed	SPFM: DC needed	λ latent-capable (FIT)	Latent DC assumed	LFM: DC needed
U14	F29P329SM-Q1 MCU	43.50	33.00	98.2%	**99.4%**	10.50	90.0%	**37.0%**
U7	DRV8263-Q1 EPB driver	20.00	2.40	90.0%	**not reachable**	6.80	72.4%	**0.0%**
U3	TPS653860-Q1 PMIC	10.80	1.20	90.0%	**not reachable**	5.60	90.0%	**0.0%**
U5	DRV3263-Q1 (CUTOFF1)	1.80	0.00	—	—	0.90	90.0%	**0.0%**
U6	WSS001-Q1	7.50	7.50	99.0%	**not reachable**	0.00	—	—
U2	LM68645-Q1 12 V buck	2.00	2.00	90.0%	**not reachable**	0.00	—	—

DC needed = the lowest coverage of that IC's violating faults at which the goal still meets its target, with every other value as assumed. A 0 % need means the IC has margin on its own. Ask TI for the FMEDA and safety manual of each IC (OQ-007, OQ-008).

Scenarios

VerB as built — Published hardware (R58 fitted, PMIC SAFE_OUT1 unconnected, no EPB terminal readback). Software safety mechanisms the hardware allows are credited as the DFMEA specifies them (ASSUMED, OQ-032).

With DFMEA actions — R58, Q6, R53 and C63 not fitted (EPB-401, EPB-404, EPB-406), SAFE_OUT1 pulls U7 nSLEEP low (EPB-408), 10 kOhm DRVOFF pull-up (EPB-121), OUTA/OUTB voltage readback (EPB-211, EPB-314), periodic cut-off test (EPB-411); for SG-01, U5 input pull resistors (BLD-102), SAFE_OUT1 also to U5 nSLEEP (BLD-120), motor-phase isolation driven independently of U5 (BLD-201, BLD-118), angle-input pull-downs (ANG-101), split ADC modules and a reference check (ANG-306, PMC-201); for SG-05, a WSSO pull-down at U14.31 (WSS-302); for SG-02,

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-01 · Computed (Rev A, provisional)

ASIL D

Avoid braking at a wheel that was not requested (unintended, excessive, misdirected or unreleased clamp force)

Safe state: Clamp force released at that wheel; corner reported unavailable; driver warned

FTTI: TBD; provisional 100 ms (ASSUMED) · Hazardous events: HE-01 to HE-06, HE-19 (S10-QLN-HARA-001 Rev B)

	SPFM · target ≥ 99%	LFM · target ≥ 90%	PMHF (FIT) · item < 10 FIT; corner share open (OQ-046)
As built	87.47%	97.05%	41.38
With actions	97.36%	96.81%	9.90

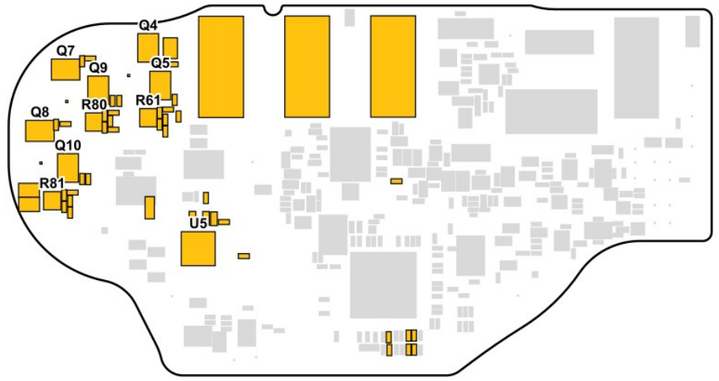
Key findings

1. As built, a shorted inverter FET (6 × 40 % of 10 FIT) is the dominant single-point fault: after the U5 stop the shorted phase and the body diodes of the other legs brake the motor, so the caliper cannot self-release on time, and VerB has no way to disconnect the motor (BLD-201). U5 die faults that drive on their own (BLD-118, BLD-227) have no stop that avoids U5. Direction: phase isolation driven independently of U5, SAFE_OUT1 to nSLEEP, defined reset-state pulls (BLD-102, BLD-120, BLD-201).

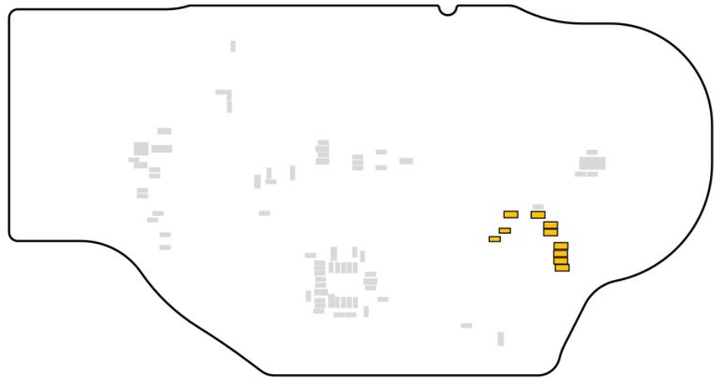
2. The angle and current checks that most rows lean on are software the DFMEA asks for but VerB does not specify (OQ-032, OQ-038), and faults common to both angle channels or to both current and angle readings (LDO1/LDO3 drift inside the monitor window, a shared ADC module or reference) have no detection as built (MCU-302, ANG-306).

3. Even with the actions every credited reaction only stops torque; the SG-01 safe state (force released) then depends on A-08 and on the unpowered release time, which is not known (OQ-023, OQ-034). If the caliper does not release within 100 ms, most of the coverage below falls away.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Elements that can build, hold or fail to release service-brake clamp force at this wheel: the BLDC gate driver U5 and its support passives, the inverter FETs (Q4, Q5, Q7-Q10), their gate pull-downs and the phase pads J7-J9, the phase-current path (shunts R61/R80/R81, the Kelvin and CSA filter network, the ADC reference network, and the IMON and DC_BUS pins that can overdrive the ADC), the angle sensors U12/U13 and their front ends, the parts of the MCU (U14) that compute and issue the torque command and receive the CAN request, the PMIC (U3) supervision and the rails that can corrupt U14, U5 or the sensors (U4 1.25 V core with its dividers, LDO1 3.3 V, LDO3 3.3Vref, U2 12 V with its feedback and VMON dividers), the 12 V overvoltage cut-off path (U1, Q1/Q2, U8/U10 INH), the MCU clock Y1, the ERRORSTS path to the PMIC, and the pedal fail-back inputs (HE-19). Other functions of U14, U3 and U5 (EPB, wheel speed, CAN housekeeping, other rails, CUTOFF1/2) are n/a here and counted on their own goals. Rail decoupling capacitors are left out: a short collapses the rail and resets the corner, which is counted under SG-02 (as SG-05 does). Common causes outside the parts list (magnet slip, stray field, PCB leakage and CAF, variant fitting of R22, R51, R146) are in the dependent-failure analysis, not here. No mechanism on VerB actively releases a clamp force built by a hardware fault: every stop relies on the caliper releasing unpowered (A-08, OQ-023; DFMEA PMC-419).

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F01-001	U5	DRV3263-Q1	Input logic or state-machine fault drives the inverter regardless of DRVOFF, nSLEEP and PWM inputs	Torque and clamp force without a request (FE-01)	U5		30.00	4%	1.200	**Direct**			**1.200**	·	·	·	**Direct**	**SM-11**	90%	·	**0.120**	·	1.080			BLD-118	As built U14 can see the current (SM-10) but its only reactions, DRVOFF and nSLEEP, act inside the failed die: not credited. With the actions U14 opens the phase isolation, which does not act through U5 (STOP).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-023
F01-002	U5	DRV3263-Q1	One gate-drive output stage stuck on (source stuck, sink lost): FET held on whatever U5 is commanded	Torque in a fixed direction during commutation, then braked release (FE-01, FE-02)	U5		30.00	6%	1.800	**Direct**			**1.800**	·	·	·	**Direct**	**SM-11**	90%	·	**0.180**	·	1.620			BLD-227, BLD-108	Every VerB reaction (gates off, DRVOFF, nSLEEP, PMIC reset) acts through U5 and cannot turn off a stuck output. With the actions the phase isolation disconnects the motor (STOP).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-023
F01-003	U5	DRV3263-Q1	DRVOFF or nSLEEP input no longer disables the gate drivers	Stop path used by the software checks lost (latent)	U5		30.00	6%	1.800	Latent	LM-11	90%	·	·	0.180	1.620	Latent	LM-11	90%	·	·	0.180	1.620	F01-004, F01-005, F01-030, F01-032, F01-	70.39	BLD-103, BLD-105	Partner: the faults whose reaction is DRVOFF high or nSLEEP low.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F01-004	U5	DRV3263-Q1	Current-sense amplifier gain, offset or output wrong (one phase or all three), or VREF input fault	Force from torque above request (FE-03)	U5		30.00	10%	3.000	**Direct**	SM-12	60%	·	**1.200**	·	1.800	**Direct**	SM-12	80%	·	**0.600**	·	2.400			BLD-312, BLD-313, BLD-320, BLD-520	A common gain error on all three phases passes the sum check; as built only force-versus-position plausibility sees it (BLD-315). STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-005	U5	DRV3263-Q1	Register corruption changes the drive configuration (PWM mode, dead time, CSA gain, protection) without a valid write	Uncontrolled or excess torque (FE-01, FE-03)	U5		30.00	4%	1.200	**Direct**	SM-13	80%	·	**0.240**	·	0.960	**Direct**	SM-13	80%	·	**0.240**	·	0.960			BLD-115, BLD-313	Detected by the cyclic readback; reaction DRVOFF and nSLEEP (U5 still obeys its inputs for this mode). STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F01-006	U5	DRV3263-Q1	VDS or Rsense overcurrent comparators, or their nFAULT report, lost or wrong	Trigger of the phase isolation lost (latent, scenario B)	U5		30.00	12%	3.600	Safe			·	·	·	·	**Latent**	**LM-10**	60%	·	·	1.440	2.160	F01-002, F01-020	25.80	BLD-222, BLD-226	As built the VDS monitor serves no credited SG-01 mechanism (it cannot remove the braking of a shorted phase), so its loss is Safe. With the actions it triggers SM-11 for FET shorts.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-007	U5	DRV3263-Q1	Outputs off or high impedance, GVDD, charge pump or internal supply fault, thermal shutdown and other faults that stop the drive	No SG-01 effect (torque lost: SG-02)	U5		30.00	52%	15.600	Safe			·	·	·	·	Safe			·	·	·	·			BLD-501, BLD-525		λ GATED OQ-007; share JUDGMENT
F01-008	U5	DRV3263-Q1	CUTOFF1 and CUTOFF2 channels	Not counted for SG-01	U5		30.00	6%	1.800	n/a			·	·	·	·	n/a			·	·	·	·				CUTOFF1 drives the EPB cut-off and is counted under SG-03; CUTOFF2 is unused on VerB (BLD-120).	λ GATED OQ-007; share JUDGMENT
F01-009	U5 support passives	C62, C64, C65, C67, C69, C72, C77, R64, R65, R68, R59, R62, R141, R143	Open, short or drift of GVDD, charge-pump and bootstrap parts, SPI series resistors and the nFAULT pull-up	No SG-01 effect (gate drive lost, or SPI frames invalid and rejected)	U5-PAS		5.60	100%	5.600	Safe			·	·	·	·	Safe			·	·	·	·			BLD-114, BLD-501	An open SPI resistor gives all-ones or all-zero frames, which the SM-13 range check rejects (BLD-114). C63, R53 and R54 (EPB option path) are counted under SG-03.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-010	R50, R55, R66, R67, R72, R73	0 Ohm 0402 gate links	Open	No SG-01 effect (the gate pull-down holds the FET off)	RES-0R	6	0.60	100%	0.600	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-020	Q4, Q5, Q7-Q10	SQJA90EP	Drain-source short	After the U5 stop the shorted phase brakes the motor: release slowed or prevented (FE-02)	FET-80V	6	60.00	40%	24.000	**Direct**			**24.000**	·	·	·	**Direct**	**SM-11**	90%	·	**2.400**	·	21.600			BLD-201, BLD-212	The U5 VDS monitor ends the shoot-through but cannot remove the braking torque, and VerB cannot disconnect the motor: no credit as built. Class Direct assumes the braked release misses the FTTI (OQ-023, OQ-034, OQ-048); if it does not, these rows are Safe. With the actions the phase isolation frees the motor (STOP).	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-023
F01-021	Q4, Q5, Q7-Q10	SQJA90EP	Drain-source open, gate-source short, on-resistance increase	No SG-01 effect (phase lost or weak: SG-02; heating: SG-07)	FET-80V	6	60.00	60%	36.000	Safe			·	·	·	·	Safe			·	·	·	·			BLD-203, BLD-210		λ JUDGMENT OQ-010; share JUDGMENT (class split)
F01-022	R52, R56, R69, R70, R74, R75	100 kOhm 0402 gate-source pull-downs	Open: FET gate undefined when U5 is not driving	Reset or sleep stop no longer holds that FET off (latent)	RES-0402	6	1.80	60%	1.080	Latent			·	·	1.080	·	Latent			·	·	1.080	·	F01-060, F01-061, F01-130	41.40	BLD-218	Matters when the stop puts U5 in reset, sleep or brown-out (SM-01, SM-02 reactions). No test exists (BLD-218 asks for a release-time measurement only).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-023	R52, R56, R69, R70, R74, R75	100 kOhm 0402 gate-source pull-downs	Short or drift	No SG-01 effect (short holds the FET off)	RES-0402	6	1.80	40%	0.720	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-024	J7, J8, J9	Motor phase wire pads	Open (crack, lift)	No SG-01 effect (phase lost: SG-02)	PAD	3	1.50	70%	1.050	Safe			·	·	·	·	Safe			·	·	·	·			BLD-212		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F01-025	J7, J8, J9	Motor phase wire pads	Short to an adjacent phase pad or to the harness	Motor windings shorted: braked release (FE-02)	PAD	3	1.50	30%	0.450	**Direct**			**0.450**	·	·	·	**Direct**			**0.450**	·	·	·			BLD-212, PCB-102	A phase-to-phase short sits on the motor side of any phase isolation, so no on-board reaction frees the motor. Same OQ-023, OQ-034, OQ-048 dependency as F01-020.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-026	Bus capacitors	C60, C73, C74, C61, C75, C76, C68	Short, open, capacitance loss or ESR rise on 48V/12V_P	No SG-01 effect (short: U1 breaker removes the corner; open: ripple only)	BUS-CAP		16.00	100%	16.000	Safe			·	·	·	·	Safe			·	·	·	·			SUP-231, PCB-202	Shorts are rated for SG-07 in PCB-202.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-030	R61, R80, R81	0.5 mOhm shunt BVN-Z	Resistance drift (one phase reads wrong)	Force from torque above request (FE-03)	SHUNT	3	3.00	70%	2.100	**Direct**	SM-12	60%	·	**0.840**	·	1.260	**Direct**	SM-12	80%	·	**0.420**	·	1.680			BLD-306	One phase off: the three-shunt sum check sees it. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F01-031	R61, R80, R81	0.5 mOhm shunt BVN-Z	Open	No SG-01 effect (low-side path lost, CMPSS and Rsense trip: drive stops)	SHUNT	3	3.00	30%	0.900	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-032	CSA front end	R60, R63, R78, R79, R82, R83, R71, R76, R77, C66, C70, C71, C78-C82, C84-C87	Open, short or drift of a Kelvin, filter or SOx part: one phase reads 0 A, offset, frozen or noisy	Force from torque above request (FE-03)	CSA-FE		8.20	70%	5.740	**Direct**	SM-12	60%	·	**2.296**	·	3.444	**Direct**	SM-12	80%	·	**1.148**	·	4.592			BLD-301 to BLD-304, BLD-307, BLD-309, BLD-319	Single-phase errors: sum check and voltage model. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F01-033	CSA front end	R60, R63, R78, R79, R82, R83, R71, R76, R77, C66, C70, C71, C78-C82, C84-C87	Faults without a reading error (filter capacitance loss within the error budget, drift within tolerance)	No SG-01 effect	CSA-FE		8.20	30%	2.460	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-034	R18, R132	7.5 kOhm IMON, 1 kOhm DC_BUS 0402	Open: IMON or DC_BUS pin driven above VDDA, ADC-A reference disturbed	Phase-current and angle readings on the same ADC wrong (FE-03)	RES-0402	2	0.60	60%	0.360	**Direct**	SM-12	60%	·	**0.144**	·	0.216	**Direct**	SM-12	80%	·	0.072	·	0.288			SUP-322, SUP-413	The pin reads full scale, which the range check flags; the disturbed phase currents fail the sum check. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F01-035	R18, R132	7.5 kOhm IMON, 1 kOhm DC_BUS 0402	Short or drift	No SG-01 effect (reading low: monitoring only)	RES-0402	2	0.60	40%	0.240	Safe			·	·	·	·	Safe			·	·	·	·				R127 is left out: open or drift only lowers the DC_BUS reading.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-036	ADC reference network	L7, L8, L10, C44, C49, C83, C116, C117, C134	Ferrite open or capacitor short: VREFHI or VDDA of one ADC group lost	All readings of that ADC group wrong (FE-03)	ADCREF-FE		5.40	50%	2.700	**Direct**	SM-12	60%	·	**1.080**	·	1.620	**Direct**	SM-12	80%	·	**0.540**	·	2.160			MCU-111, MCU-113, PMC-203	A lost reference drives the readings to the rails, which the range checks of SM-12 (and SM-14 for the angle channels) flag. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F01-037	ADC reference network	L7, L8, L10, C44, C49, C83, C116, C117, C134	Capacitor open or capacitance loss, ferrite degraded	No SG-01 effect (reference noise within the error budget)	ADCREF-FE		5.40	50%	2.700	Safe			·	·	·	·	Safe			·	·	·	·			PMC-209	Ripple above the budget is PMC-209; not credited here.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-040	U12	TMAG6180-Q1	SIN/COS in range but wrong (offset, gain, phase) or quadrant outputs wrong	Commutation angle wrong: torque and force not as commanded (FE-03, FE-02)	U12-U13		10.00	50%	5.000	**Direct**	SM-14	90%	·	**0.500**	·	4.500	**Direct**	SM-14	97%	·	**0.150**	·	4.850			ANG-102, ANG-103, ANG-104	U12 is taken as the commutation channel (ASSUMED, OQ-038). STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-041	U12	TMAG6180-Q1	Output stuck at a rail or out of the 10-90 % band	Commutation angle wrong (FE-03)	U12-U13		10.00	15%	1.500	**Direct**	SM-14	90%	·	**0.150**	·	1.350	**Direct**	SM-14	97%	·	0.045	·	1.455			ANG-107, ANG-108	Range check within one sample. STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-042	U12	TMAG6180-Q1	Internal diagnostic puts U12 in its safe state: outputs Hi-Z and held in range on C110/C111	Channel-1 angle frozen at a plausible value (FE-02)	U12-U13		10.00	20%	2.000	**Direct**	SM-14	90%	·	**0.200**	·	1.800	**Direct**	SM-14	97%	·	0.060	·	1.940			ANG-101, ANG-119	As built only the channel compare sees it, once the rotor moves (no pull-downs). With the actions the ANG-101 pull-downs move the node out of range within about 2 ms. STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-043	U12	TMAG6180-Q1	Faults without an output error (supply current, internal redundancy)	No SG-01 effect	U12-U13		10.00	15%	1.500	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F01-044	U13	TMAG6180-Q1	Output wrong in range, stuck, frozen (Hi-Z) or quadrant wrong	Monitor channel of the angle compare lost (latent)	U12-U13		10.00	85%	8.500	Latent	LM-12	90%	·	·	0.850	7.650	Latent	LM-12	97%	·	·	0.255	8.245	F01-040, F01-041, F01-042, F01-050	11.09	ANG-201 to ANG-213	U13 is only compared, not used for commutation (ASSUMED, OQ-038); a U13 fault shows as a mismatch at the next movement.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-045	U13	TMAG6180-Q1	Faults without an output error	No SG-01 effect	U12-U13		10.00	15%	1.500	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F01-050	Angle front end ch1	R119, R121, R120, R122, C109, C110, C111, J21	Open, short or drift on SIN_P1/COS_P1, Q01/Q11 or the U12 supply pin	Channel-1 angle wrong, frozen or 180 deg off (FE-03, FE-02)	ANG-FE		3.70	70%	2.590	**Direct**	SM-14	90%	·	**0.259**	·	2.331	**Direct**	SM-14	97%	·	0.078	·	2.512			ANG-103, ANG-107 to ANG-111, ANG-120,	An open R119/R121 leaves the ADC input held on the filter (ANG-109): compare only. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F01-051	Angle front end ch1	R119, R121, R120, R122, C109, C110, C111, J21	Faults within the error budget (decoupling open, small drift)	No SG-01 effect	ANG-FE		3.70	30%	1.110	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-052	Angle front end ch2	R123, R125, R124, R126, C112, C113, C114, J22	Open, short or drift on SIN_P2/COS_P2, Q02/Q12 or the U13 supply pin	Monitor channel of the angle compare lost (latent)	ANG-FE		3.70	70%	2.590	Latent	LM-12	90%	·	·	0.259	2.331	Latent	LM-12	97%	·	·	0.078	2.512	F01-040, F01-041, F01-042, F01-050	11.09	ANG-205 to ANG-212		λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F01-053	Angle front end ch2	R123, R125, R124, R126, C112, C113, C114, J22	Faults within the error budget	No SG-01 effect	ANG-FE		3.70	30%	1.110	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-060	U14	F29P329SM-Q1	CPU, memory or bus fault produces a wrong torque or force command	Torque and clamp force without or above request (FE-01, FE-03)	U14		150.00	25%	37.500	**Direct**	SM-01	99%	·	**0.375**	·	37.125	**Direct**	SM-01	99%	·	**0.375**	·	37.125			BLD-101, MCU-503	Lockstep error resets U14. As built the drive then stops only if U5 treats floating DRVOFF/nSLEEP/PWM inputs as off (unpublished internal pulls, BLD-102): ASSUMED, OQ-007. With the actions the BLD-102 pulls and SAFE_OUT1 put U5 to sleep. STOP.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-061	U14	F29P329SM-Q1	Fault common to both lockstep cores (internal clock, core supply, reset logic) that upsets program flow	Wrong or frozen command (FE-01, FE-02)	U14		150.00	2%	3.000	**Direct**	SM-02	90%	·	**0.300**	·	2.700	**Direct**	SM-02	90%	·	**0.300**	·	2.700			MCU-507, MCU-112	The lockstep cannot see a fault common to both cores; the Q&A watchdog on its own time base sees the disturbed answer sequence. A common fault that leaves program flow intact is not covered (it sits in the 1 - DC). STOP, through the reset as F01-060.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-002
F01-062	U14	F29P329SM-Q1	BLDC PWM output pins (U14.88-93) stuck or shorted (port fault the lockstep does not see)	Phase switched without a command (FE-01)	U14		150.00	2%	2.250	**Direct**	SM-10	60%	·	**0.900**	·	1.350	**Direct**	SM-10	80%	·	**0.450**	·	1.800			BLD-108, MCU-401, MCU-402	The CPU keeps running and servicing the watchdog, so SM-01 and SM-02 do not see it. SM-10 sees current with no command and asserts DRVOFF/nSLEEP on other pins (U14.87, U14.86). STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F01-063	U14	F29P329SM-Q1	DRVOFF (U14.87) or nSLEEP (U14.86) pin stuck in the enable state	Stop path used by the software checks lost (latent)	U14		150.00	1%	0.750	Latent	LM-11	90%	·	·	0.075	0.675	Latent	LM-11	90%	·	·	0.075	0.675	F01-004, F01-005, F01-030, F01-032, F01-	32.89	BLD-103, BLD-105, BLD-120		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F01-064	U14	F29P329SM-Q1	ADC channel, multiplexer or sample-and-hold fault on a phase-current input	Force from torque above request (FE-03)	U14		150.00	2%	2.250	**Direct**	SM-12	60%	·	**0.900**	·	1.350	**Direct**	SM-12	80%	·	**0.450**	·	1.800			MCU-111, MCU-307	Single-channel error: sum check. STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-065	U14	F29P329SM-Q1	ADC channel fault on one angle input	Commutation angle wrong (FE-03)	U14		150.00	1%	1.500	**Direct**	SM-14	90%	·	**0.150**	·	1.350	**Direct**	SM-14	97%	·	0.045	·	1.455			MCU-308, MCU-309	STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-066	U14	F29P329SM-Q1	ADC module or reference fault common to both angle channels (both converted on one module)	Same angle error on both channels: the compare agrees (FE-03)	U14		150.00	1%	1.500	**Direct**			**1.500**	·	·	·	**Direct**	**SM-15**	80%	·	**0.300**	·	1.200			ANG-306, MCU-118	No detection as built. With the actions the channels move to different ADC modules and a known reference is converted each cycle. STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-067	U14	F29P329SM-Q1	MCAN peripheral or message-RAM fault delivers a wrong, stale or misaddressed clamp-force request	Force built on a request that was not sent to this wheel (FE-01, FE-02, FE-04)	U14		150.00	1%	1.500	**Direct**	SM-16	90%	·	**0.150**	·	1.350	**Direct**	SM-16	90%	·	**0.150**	·	1.350			MCU-508, CAN-102, CAN-131, CAN-209	Message-RAM ECC covers storage; E2E covers the whole receive path. REL (U14 and U5 are healthy for this mode).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-040

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F01-068	U14	F29P329SM-Q1	Lockstep comparator, ECC or error-signal module fault	MCU self-monitoring blind (latent)	U14		150.00	5%	7.500	Latent	LM-04	90%	·	·	0.750	6.750	Latent	LM-04	90%	·	·	0.750	6.750	F01-060	37.50	MCU-504, MCU-505, MCU-506		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-069	U14	F29P329SM-Q1	Other MCU functions (EPB, wheel speed, pedal SENT capture, other peripherals)	Not counted for SG-01	U14		150.00	62%	92.250	n/a			·	·	·	·	n/a			·	·	·	·				Excluded rather than counted as safe, as on SG-03. The pedal capture share is covered by the pedal rows' LM-14 only.	λ GATED OQ-007; share JUDGMENT
F01-070	U3	TPS653860-Q1	Watchdog or error monitor fails to act, or NRST cannot reset the MCU	Stop path for MCU faults lost (latent)	U3		40.00	8%	3.200	Latent	LM-05	90%	·	·	0.320	2.880	Latent	LM-05	90%	·	·	0.320	2.880	F01-061, F01-130	3.90	PMC-402, PMC-404, PMC-405	The lockstep resets U14 internally (ESMRESET), so F01-060 is not a partner.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-071	U3	TPS653860-Q1	SAFE_OUT1 fails to assert in the safe state	MCU-independent U5 stop lost (latent)	U3		40.00	3%	1.200	n/a			·	·	·	·	**Latent**	**LM-05**	90%	·	·	0.120	1.080	F01-060, F01-061, F01-130	41.40	PMC-401, BLD-120	SAFE_OUT1 is unconnected on VerB. Same pin as F03-031 (it drives U5 and U7 nSLEEP with the actions).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-072	U3	TPS653860-Q1	LDO1 (3.3 V: U14 I/O, U5 logic, U12/U13) or LDO3 (3.3Vref) regulates outside its monitor window, high or low	U14, U5 and both angle sensors overdriven or browned out together; readings scaled (FE-01, FE-02, FE-03)	U3		40.00	7%	2.800	**Direct**	SM-08	90%	·	**0.280**	·	2.520	**Direct**	SM-08	90%	·	**0.280**	·	2.520			PMC-203, PMC-206, ANG-305	Rule 4 row. The monitors sit in the regulator's die; the reaction resets U14 but does not remove an overvoltage (PMC-206), and LDO1 undervoltage between 2.3 and 2.65 V freezes both angle channels unless the UV threshold is above 2.65 V (ANG-305, OQ-002). STOP.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F01-073	U3	TPS653860-Q1	LDO1 or LDO3 drifts inside the monitor window	Same angle offset on both channels, phase currents scaled (FE-03)	U3		40.00	4%	1.600	**Direct**			**1.600**	·	·	·	**Direct**	**SM-15**	80%	·	**0.320**	·	1.280			PMC-201, ANG-113, MCU-302	As built no independent reference can be converted (MCU-302): no detection. With the actions a known reference on a separate ADC module is checked each cycle. STOP.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F01-074	U3	TPS653860-Q1	Rail monitors (EXT_VMON1, LDO1, LDO3) stuck at 'good'	Supply faults no longer detected (latent)	U3		40.00	3%	1.200	Latent	LM-05	90%	·	·	0.120	1.080	Latent	LM-05	90%	·	·	0.120	1.080	F01-072, F01-080, F01-081, F01-083	5.53	PMC-214, PMC-312, PMC-317		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F01-075	U3	TPS653860-Q1	Spurious reset or safe state	No SG-01 effect (corner off, reported: SG-02)	U3		40.00	10%	4.000	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F01-076	U3	TPS653860-Q1	Other PMIC functions (buck-boost, LDO2, PLDO1/2 pedal supplies, EPB-related, rails lost)	Not counted for SG-01	U3		40.00	65%	26.000	n/a			·	·	·	·	n/a			·	·	·	·				Loss of a rail resets U14 and stops the drive (SG-02). Rails running high are F01-072 and the U4 rows.	λ GATED OQ-007; share JUDGMENT
F01-080	U4	TPS62902-Q1	1.25 V core regulated high (half of TI's 'output out of specification' mode)	U14 core overdriven: erratic commands, common to both lockstep cores (FE-01)	U4		12.00	11%	1.320	**Direct**	SM-08	90%	·	**0.132**	·	1.188	**Direct**	SM-08	90%	·	**0.132**	·	1.188			PMC-303, PMC-315	EXT_VMON1 resets U14; the source stays (PMC-303). STOP. Half-and-half split as F03-110.	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F01-081	U4	TPS62902-Q1	High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	U14 core overdriven (FE-01)	U4		12.00	10%	1.200	**Direct**	SM-08	90%	·	**0.120**	·	1.080	**Direct**	SM-08	90%	·	**0.120**	·	1.080			PMC-301, PMC-302, PMC-304	PMC-304: the monitor may act after the U14 absolute maximum (about 1 us slew). Credit kept as SM-08 is defined; see the proposed notes. STOP.	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F01-082	U4	TPS62902-Q1	Output low or lost, low-side stuck on, power-FET damage, power-good and enable faults	No SG-01 effect (U14 brown-out reset: drive stops)	U4		12.00	79%	9.480	Safe			·	·	·	·	Safe			·	·	·	·			PMC-306, PMC-307, PMC-308	Safe as built only if U5 treats floating inputs as off (BLD-102, as F01-060). TI SFFS465A split less the two rows above.	λ JUDGMENT OQ-010
F01-083	R46, R48	107 kOhm, 100 kOhm 0402 (U4 feedback)	R46 open or R48 short: feedback at 0 V, U4 drives the core high	U14 core overdriven (FE-01)	RES-0402	2	0.60	35%	0.210	**Direct**	SM-08	90%	·	0.021	·	0.189	**Direct**	SM-08	90%	·	0.021	·	0.189			PMC-301	EXT_VMON1 has its own divider (R44/R47), so it sees this. Share: (R46 open 0.60 + R48 short 0.10) / 2. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC GATED OQ-002
F01-084	R46, R48	107 kOhm, 100 kOhm 0402 (U4 feedback)	R46 short, R48 open, drift within tolerance	No SG-01 effect (core low: brown-out reset)	RES-0402	2	0.60	65%	0.390	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-085	R44, R47	16.2 kOhm, 15 kOhm 0402 (EXT_VMON1 divider)	Drift: core monitor threshold shifted	Core overvoltage detected late or not at all (latent)	RES-0402	2	0.60	30%	0.180	Latent			·	·	0.180	·	Latent			·	·	0.180	·	F01-080, F01-081, F01-083	2.73	PMC-312, PMC-314	No test of the divider exists (PMC-314).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-086	R44, R47	16.2 kOhm, 15 kOhm 0402 (EXT_VMON1 divider)	Open or short	No SG-01 effect (monitor input at 0 V or 1.25 V: UV or OV trip, corner off)	RES-0402	2	0.60	70%	0.420	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-090	R134, R136	1 kOhm, 10 kOhm 0402 (ERRORSTS)	Open: GPI1 held at the no-error level or floating	PMIC escalation of U14 errors lost (latent)	RES-0402	2	0.60	60%	0.360	Latent	LM-05	90%	·	·	0.036	0.324	Latent	LM-05	90%	·	·	0.036	0.324	F01-061, F01-130	3.90	PMC-409, MCU-515	The start-up forced-error test (LM-05 with MCU-504) sees it.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F01-091	R134, R136	1 kOhm, 10 kOhm 0402 (ERRORSTS)	Short or drift	No SG-01 effect	RES-0402	2	0.60	40%	0.240	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-100	U2	LM68645-Q1	High-side FET short: 12 V rail pulled toward 48V/12V_P	U5 GVDD and PMIC input overdriven: gate drive and rails out of control (FE-01)	U2		20.00	10%	2.000	**Direct**	SM-09	90%	·	**0.200**	·	1.800	**Direct**	SM-09	90%	·	**0.200**	·	1.800			BCK-101, PMC-102, BLD-505	Rule 4 row. SM-09 removes 48V/12V_P in about 2 ms, which also unpowers the inverter (STOP), but the 12 V loads may already be overstressed (BCK-101) and the cut-off is not latched (OQ-041). Same split as F03-120.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-014
F01-101	U2	LM68645-Q1	Output low or lost, regulation faults within the PMIC input range	No SG-01 effect (gate drive or PMIC input lost: drive stops)	U2		20.00	90%	18.000	Safe			·	·	·	·	Safe			·	·	·	·			BCK-106, PMC-104		λ GATED OQ-007; share JUDGMENT
F01-102	R33, R35	100 kOhm, 7.15 kOhm 0402 (U2 feedback)	R33 open or R35 short: feedback at 0 V, U2 drives 12 V toward the input	U5 GVDD and PMIC input overdriven (FE-01)	RES-0402	2	0.60	35%	0.210	**Direct**	SM-09	90%	·	0.021	·	0.189	**Direct**	SM-09	90%	·	0.021	·	0.189			BCK-201, BCK-202	The U2 VSNS overvoltage protection is not credited (its Q3 reaction cannot hold, BCK-101); SM-09 is. Share as F01-083. STOP.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F01-103	R33, R35	100 kOhm, 7.15 kOhm 0402 (U2 feedback)	R33 short, R35 open, drift within tolerance	No SG-01 effect (12 V low)	RES-0402	2	0.60	65%	0.390	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-104	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Drift: VMON reads 12 V low	12 V overvoltage cut-off acts late or not at all (latent)	RES-0402	2	0.60	30%	0.180	Latent			·	·	0.180	·	Latent			·	·	0.180	·	F01-100, F01-102	2.21	MCU-306, BCK-206	The CMPSS DAC-code test of LM-13 tests the comparator, not the divider scale.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-105	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Open or short	No SG-01 effect (VMON at 0 V or clamped high: CMPSS window trips, corner off)	RES-0402	2	0.60	70%	0.420	Safe			·	·	·	·	Safe			·	·	·	·			MCU-306		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-110	U1	LM74930-Q1	HGATE stuck high (TI 5 %): Q1 cannot be turned off	Reaction of SM-09 lost (latent)	U1		14.00	5%	0.700	Latent	LM-13	60%	·	·	0.280	0.420	Latent	LM-13	60%	·	·	0.280	0.420	F01-100, F01-102	2.21	SUP-209, SUP-211, SUP-404	SG-03 counts all U1 modes Safe (F03-125); here the stuck HGATE defeats the SM-09 cut-off, so it is latent. TI SFFS950 split.	DC PROVISIONAL OQ-014
F01-111	U1	LM74930-Q1	IMON fault (TI 5 %): IMON drives U14.35 above the ADC range	ADC-A reference disturbed: phase-current and angle readings wrong (FE-03)	U1		14.00	5%	0.700	**Direct**	SM-12	60%	·	**0.280**	·	0.420	**Direct**	SM-12	80%	·	**0.140**	·	0.560			SUP-322, SUP-325	Counted whole: TI does not split a high IMON from a low one. STOP.	DC PROVISIONAL OQ-038
F01-112	U1	LM74930-Q1	DGATE modes, HGATE out of spec or stuck low, OCP, SCP, UV/OV, pin-to-pin short (TI 40 + 26 + 11 + 8 + 5 %)	No SG-01 effect (48V/12V_P lost, or a protection against external surges lost)	U1		14.00	90%	12.600	Safe			·	·	·	·	Safe			·	·	·	·			SUP-305, SUP-311, SUP-401	An external surge is not a random hardware fault of this ECU (as F03-125).	
F01-113	Q1, Q2	SQJA90EP	Q1 drain-source short (40 % of Q1)	Reaction of SM-09 lost (latent)	FET-80V	2	20.00	20%	4.000	Latent	LM-13	60%	·	·	1.600	2.400	Latent	LM-13	60%	·	·	1.600	2.400	F01-100, F01-102	2.21	SUP-203, SUP-208	Share of the Q1/Q2 pair.	λ JUDGMENT OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F01-114	Q1, Q2	SQJA90EP	Q1 other modes; any Q2 mode (reverse blocking)	No SG-01 effect (supply lost, or reverse protection lost)	FET-80V	2	20.00	80%	16.000	Safe			·	·	·	·	Safe			·	·	·	·					λ JUDGMENT OQ-010; share JUDGMENT
F01-115	U8, U10	TCAN1043H-Q1	Transceiver stays awake when nSTB_CAN goes low (INH held high)	Reaction of SM-09 lost (latent)	TCAN	2	18.00	2%	0.360	Latent	LM-13	60%	·	·	0.144	0.216	Latent	LM-13	60%	·	·	0.144	0.216	F01-100, F01-102	2.21	CAN-119, CAN-408, CAN-412	Same share as F03-151 (part of TI's 5 % pin-short mode). Here the key-off cut-off test of CAN-408 is credited as LM-13.	share JUDGMENT; DC PROVISIONAL OQ-014

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F01-116	U8, U10	TCAN1043H-Q1	Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	No SG-01 effect (one bus lost: requests arrive on the other; both lost: timeout releases, SG-02)	TCAN	2	18.00	98%	17.640	Safe			·	·	·	·	Safe			·	·	·	·			CAN-102, CAN-104, CAN-201	A transceiver cannot create a CRC-valid request. Also the event that activates the pedal fall-back (partner of F01-140 and F01-142).	share JUDGMENT
F01-117	INH network	D6, D7, R102, R112, R156, R19, R26, R36	R156 open: INH_CAN floats instead of going low	Reaction of SM-09 lost (latent)	INH-NET		3.80	5%	0.190	Latent	LM-13	60%	·	·	0.076	0.114	Latent	LM-13	60%	·	·	0.076	0.114	F01-100, F01-102	2.21	CAN-409	0.3 FIT × 60 % open of 3.8 FIT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F01-118	INH network	D6, D7, R102, R112, R156, R19, R26, R36	Other faults (diode open or short, series resistors)	No SG-01 effect (INH low: corner off; or one transceiver's INH path lost, the other holds it)	INH-NET		3.80	95%	3.610	Safe			·	·	·	·	Safe			·	·	·	·			SUP-405		λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-130	Y1	CDC6C-Q1	Wrong frequency or poor accuracy	U14 timebase wrong: control loop and PWM timing wrong (FE-03)	Y1		3.00	30%	0.900	**Direct**	SM-02	90%	·	0.090	·	0.810	**Direct**	SM-02	90%	·	0.090	·	0.810			MCU-203	The PMIC Q&A watchdog runs on its own time base, so a wrong U14 frequency breaks the window (TI SFFS685 split). STOP, through the reset as F01-060.	DC PROVISIONAL OQ-002
F01-131	Y1	CDC6C-Q1	No output clock, or clock degraded (jitter, duty cycle)	No SG-01 effect (missing-clock detection resets U14; degraded clock stays within the PLL range)	Y1		3.00	70%	2.100	Safe			·	·	·	·	Safe			·	·	·	·			MCU-201, MCU-202	Safe as built only with the BLD-102 assumption of F01-060.	
F01-132	R137	33 Ohm 0402	Open, short or drift of the clock series resistor	No SG-01 effect (open: clock lost, U14 reset)	RES-0402		0.30	100%	0.300	Safe			·	·	·	·	Safe			·	·	·	·			MCU-202		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-140	Pedal input networks	Force: R1, R3, R5, R128, R145, C1, C3; travel: R2, R4, R6, R129, R144, C2, C4	Open, short or drift: pedal value offset, scaled, stuck or following another channel	Wrong fall-back demand, acted on once the CAN request is lost (latent, HE-19)	PED-FE	2	4.20	70%	2.940	Latent	LM-14	60%	·	·	1.176	1.764	Latent	LM-14	60%	·	·	1.176	1.764	F01-116	17.64	PED-103 to PED-121, PED-204 to PED-222	Latent because the fall-back is used only when the requests stop; partner: the transceiver faults that stop them (a proxy: the brake controller's own loss of requests is outside this ECU).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-009
F01-141	Pedal input networks	Force: R1, R3, R5, R128, R145, C1, C3; travel: R2, R4, R6, R129, R144, C2, C4	Faults without a value error (filter capacitance loss, drift within the SENT timing budget)	No SG-01 effect	PED-FE	2	4.20	30%	1.260	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-142	J11-J16	Pedal sensor wire pads	Open or short to an adjacent pad (signal, supply or ground)	Wrong fall-back demand (latent, HE-19)	PAD	6	3.00	100%	3.000	Latent	LM-14	60%	·	·	1.200	1.800	Latent	LM-14	60%	·	·	1.200	1.800	F01-116	17.64	PED-104, PED-204, PED-205, PED-303.	An open signal wire reads only 4.5 % of span above the valid band (PED-104): part of LM-14's 1 - DC.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-009
F01-150	New (BLD-102)	U5 input pulls: DRVOFF pull-up, nSLEEP pull-down, nCS pull-up, 6 PWM pull-downs	Open of the DRVOFF pull-up or the nSLEEP pull-down: U5 not held off while U14 is in reset	Reset-based stop for MCU faults lost (latent)	RES-0402	9	2.70	13%	0.351	n/a			·	·	·	·	**Latent**	**LM-11**	90%	·	·	0.035	0.316	F01-060, F01-061, F01-130	41.40	BLD-102	2 of 9 resistors × 60 % open.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-032
F01-151	New (BLD-102)	U5 input pulls: DRVOFF pull-up, nSLEEP pull-down, nCS pull-up, 6 PWM pull-downs	Other modes (PWM or nCS pulls, shorts, drift)	No SG-01 effect (the nSLEEP pull-down alone puts U5 to sleep; a short holds U5 off)	RES-0402	9	2.70	87%	2.349	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F01-152	New (BLD-120)	1 kOhm nSLEEP series resistor	Short: SAFE_OUT1 cannot override the U14 drive on nSLEEP	MCU-independent U5 stop lost (latent)	RES-0402		0.30	10%	0.030	n/a			·	·	·	·	**Latent**	**LM-05**	90%	·	·	0.003	0.027	F01-060, F01-061, F01-130	41.40	BLD-120		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F01-153	New (BLD-120)	1 kOhm nSLEEP series resistor	Open or drift	No SG-01 effect (open: U5 sleeps)	RES-0402		0.30	90%	0.270	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-154	New (ANG-101)	100 kOhm SIN/COS pull-downs at U14	Open: a Hi-Z sensor output is held in range again	Fast detection of a sensor in its safe state lost (latent)	RES-0402	4	1.20	60%	0.720	n/a			·	·	·	·	**Latent**			·	·	0.720	·	F01-042	2.00	ANG-101, ANG-201	The channel compare still sees the frozen channel once the rotor moves; nothing tests the pull-down itself.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-155	New (ANG-101)	100 kOhm SIN/COS pull-downs at U14	Short or drift	No SG-01 effect (short: reading at 0 V, range check flags it)	RES-0402	4	1.20	40%	0.480	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F01-156	New (BLD-201)	Phase isolation FETs (back-to-back, two phases)	Drain-source short: the isolation cannot open	Reaction of SM-11 lost (latent)	FET-80V	4	40.00	40%	16.000	n/a			·	·	·	·	**Latent**	**LM-15**	90%	·	·	1.600	14.400	F01-001, F01-002, F01-020	27.00	BLD-201	Count of four FETs assumes back-to-back pairs in two phases (BLD-201 minimum); a star-point switch would change it.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F01-157	New (BLD-201)	Phase isolation FETs (back-to-back, two phases)	Open, gate-source short, on-resistance increase	No SG-01 effect (phase disconnected: SG-02)	FET-80V	4	40.00	60%	24.000	n/a			·	·	·	·	**Safe**			·	·	·	·					λ JUDGMENT OQ-010; share JUDGMENT (class split)
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**330.15 λ**			**30.550**	**10.828**	**8.506**	**102.726**	**375.55 λ**			**0.450**	**9.447**	**11.648**	**152.967**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-02 · Computed (Rev A, provisional)

ASIL C

Avoid loss of, insufficient or late braking at a wheel when braking is requested

Safe state: Corner reported unavailable or limited; other corners and regeneration compensate; driver warned

FTTI: TBD; provisional 200 ms (ASSUMED) · Hazardous events: HE-07 to HE-12 (S10-QLN-HARA-001 Rev B)

	SPFM · target ≥ 97%	LFM · target ≥ 80%	PMHF (FIT) · item < 100 FIT; corner share open (OQ-046)
As built	80.80%	98.98%	59.40
With actions	90.42%	99.16%	31.19

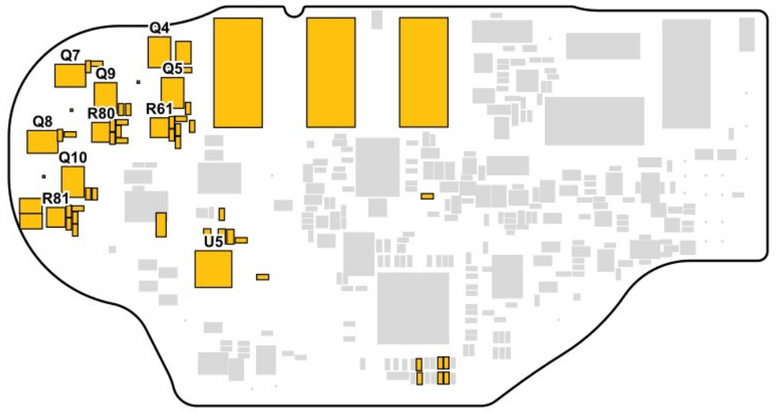
Key findings

1. SG-02 rests on one mechanism outside this ECU: the brake controller's timeout of the corner status frames (SM-30, DFMEA PMC-118). About half of the SG-02 λ (155 of 309 FIT as built) is supply, rail and reset faults that take U14 and both CAN channels down together, so the corner cannot send a last message. The timeout, its value and the reaction are not specified (OQ-022, OQ-040); it is credited at Medium in both scenarios. As built SPFM is 80.8 %; High coverage of the timeout (PMC-118 specification and HIL proof) would add about 4.5 points.

2. With the actions SG-02 reaches 90.4 % against its 97 % target on the ASSUMED data. The gap is the silent-corner faults above and the drive that stops following its command while the corner still reports "available": inverter FETs, U5 outputs and gate supply, the isolation FETs the SG-01 actions add. Only the drive-response monitor sees those (SM-31, BLD-104, BLD-202), credited at Medium with the actions. SM-30 and SM-31 both at High would give 97.2 %.

3. As built the largest single-point faults are the ones SG-01 already names: LDO1/LDO3 drift inside the PMIC window and an ADC fault common to both angle channels scale the torque at this wheel with nothing to see it (PMC-201, ANG-306, MCU-302). The actions that fix them for SG-01 (SM-15) fix them here. PMHF is about 59 FIT as built and 31 FIT with the actions for one corner; with four corners on the item budget (OQ-046) the as-built value would exceed 100 FIT.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Elements whose faults can remove, weaken or delay the clamp force at this wheel, or silence the corner without a report: the BLDC gate driver U5 and its support passives, the inverter FETs (Q4, Q5, Q7-Q10), their gate links and pull-downs, the phase pads J7-J9 and the 48 V bus capacitors; the phase-current path (shunts, CSA front end, ADC reference network, the IMON and DC_BUS pins); the angle sensors U12/U13 and their front ends; the parts of U14 that compute the torque command, drive U5, receive the request and send the corner status; the PMIC U3 (rails, monitors, watchdog, spurious resets); the whole supply chain that can silence the corner (supply pads J3/J4, the input stage and U1 with its support network, Q1/Q2, the INH path, the 12 V buck U2 and its switch Q3/Q12, the U4 core buck and its dividers, the decoupling of every logic rail, the power inductors and rail links); the MCU clock; the ERRORSTS path; and the CAN transceivers that carry both the request and the status. Other functions of U14, U3 and U5 (EPB, wheel speed, pedal supplies, CUTOFF1/2) are n/a here. The pedal fail-back is left out: it is used only after both CAN channels are lost, and then the corner is already reported by the status timeout (its own faults are rated for HE-19 on SG-01). Faults that only make the corner brake harder are SG-01 and n/a here; faults whose only effect is an available, reported corner loss (a false trip) are counted Direct with the mechanism that reports them, never Safe. The brake-controller status timeout (SM-30) sits in another ECU and is credited as an assumption of use; its own faults belong to that ECU's FMEDA.

Failure modes													VerB as built								With DFMEA actions								Traceability			
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F02-001	U5	DRV3263-Q1	Input logic or state-machine fault drives the inverter regardless of DRVOFF, nSLEEP and PWM inputs	Torque not as commanded: too little or none at this wheel (FE-05)	U5		30.00	4%	1.200	Direct	SM-31	60%	·	0.480	·	0.720	Direct	SM-31	90%	·	0.120	·	1.080			BLD-118, BLD-104	Same mode as F01-001. For SG-02 the reaction is the report, which does not need U5 to obey: U14 sees phase current not following the command and reports the corner unavailable (RPT). Stopping the drive is an SG-01 matter.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-002	U5	DRV3263-Q1	One gate-drive output stage stuck on (source stuck, sink lost)	Shoot-through at the next complementary switching; VDS trip stops the drive (FE-05)	U5		30.00	6%	1.800	Direct	SM-31	60%	·	0.720	·	1.080	Direct	SM-31	90%	·	0.180	·	1.620			BLD-227, BLD-108	Same mode as F01-002. U5 nFAULT also flags the VDS trip; SM-31 is credited because it does not depend on U5's unpublished thresholds (OQ-007). RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-003	U5	DRV3263-Q1	Current-sense amplifier gain, offset or output wrong (one phase or all three), or VREF input fault	Reading high: torque and clamp force below request (FE-05)	U5		30.00	10%	3.000	Direct	SM-12	60%	·	1.200	·	1.800	Direct	SM-12	80%	·	0.600	·	2.400			BLD-312, BLD-313, BLD-320, BLD-520	Same mode and share as F01-004; the error direction that reads high is the SG-02 half, but the mode is not split (as SG-01). A common gain error on all three phases passes the sum check (SM-12 DC). RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-004	U5	DRV3263-Q1	Register corruption changes the drive configuration (PWM mode, dead time, CSA gain, protection thresholds) without a valid write	Drive weakened, stopped by a protection, or current scaled (FE-05)	U5		30.00	4%	1.200	Direct	SM-13	80%	·	0.240	·	0.960	Direct	SM-13	80%	·	0.240	·	0.960			BLD-115, BLD-313, BLD-106	Same mode as F01-005. Cyclic readback within 100 ms, then the corner is reported unavailable (RPT).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-005	U5	DRV3263-Q1	Outputs off or high impedance, GVDD, charge-pump, bootstrap or internal-supply fault, thermal shutdown, spurious VDS/Rsense trip or false nFAULT	No torque at this wheel although braking is requested (FE-05)	U5		30.00	58%	17.400	Direct	SM-31	60%	·	6.960	·	10.440	Direct	SM-31	90%	·	1.740	·	15.660			BLD-501, BLD-503, BLD-507, BLD-509, BLD-523, BLD-525	F01-007 (0.52, Safe for SG-01) plus the spurious half of F01-006 (0.06). This is the main SG-02 mode of U5: it is silent unless U14 checks that current follows the command (BLD-104) or reads nFAULT and the SPI status (BLD-503). RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-006	U5	DRV3263-Q1	DRVOFF or nSLEEP no longer disables; VDS/Rsense protection lost; CUTOFF1 and CUTOFF2 channels	No SG-02 effect	U5		30.00	18%	5.400	n/a			·	·	·	·	n/a			·	·	·	·			BLD-103, BLD-222	F01-003 (0.06), the loss half of F01-006 (0.06) and F01-008 (0.06). The SG-02 reaction is a report and uses neither the disable inputs nor the VDS monitor, so their loss is not latent here; counted under SG-01 and SG-03.	λ GATED OQ-007; share JUDGMENT
F02-007	U5 support passives	C62, C64, C65, C67, C69, C72, C77, R64, R65, R68, R59, R62, R141, R143	GVDD, VCP or bootstrap capacitor short or open, bootstrap resistor open, DVDD or SPI series resistor open	Gate drive lost or weakened, or U5 unreachable over SPI: no or too little torque (FE-05)	U5-PAS		5.60	70%	3.920	Direct	SM-31	60%	·	1.568	·	2.352	Direct	SM-31	90%	·	0.392	·	3.528			BLD-207, BLD-208, BLD-219, BLD-502, BLD-509, BLD-510,	A C62 short pulls the 12 V rail down (BLD-502): the corner then goes silent (TMO) rather than reporting, which SM-30 covers; the row carries the more common drive-loss case. RPT. Aggregated class split, as SG-01 F01-009.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-032
F02-008	U5 support passives	C62, C64, C65, C67, C69, C72, C77, R64, R65, R68, R59, R62, R141, R143	Capacitance loss or drift within the TI requirement; nFAULT pull-up faults	No SG-02 effect	U5-PAS		5.60	30%	1.680	n/a			·	·	·	·	n/a			·	·	·	·			BLD-511, BLD-116	nFAULT is not a credited SG-02 mechanism (SM-31 is), so its pull-up is not latent here.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-009	R50, R55, R66, R67, R72, R73	0 Ohm 0402 gate links	Open	One FET never turns on: phase lost, torque low and rippled (FE-05)	RES-0R	6	0.60	100%	0.600	Direct	SM-31	60%	·	0.240	·	0.360	Direct	SM-31	90%	·	0.060	·	0.540			BLD-203	The U5 VGS monitor may not see a gate disconnected after the pin (BLD-203, OQ-007); the per-phase current check does (BLD-110). RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-020	Q4, Q5, Q7-Q10	SQJA90EP	Drain-source short, drain-source open or gate-source short	Phase lost, shorted or braking: no or too little torque (FE-05)	FET-80V	6	60.00	75%	45.000	Direct	SM-31	60%	·	18.000	·	27.000	Direct	SM-31	90%	·	4.500	·	40.500			BLD-201, BLD-202, BLD-204	Short: the U5 VDS monitor stops the drive at the first complementary switching and the shorted phase brakes the motor. Open or G-S short: one phase switch never conducts. All show as current not following the command. A short that trips the U1 breaker silences the corner instead (TMO). RPT.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-021	Q4, Q5, Q7-Q10	SQJA90EP	On-resistance increase	No SG-02 effect (the current loop raises the duty and still reaches the commanded current; heating: SG-07)	FET-80V	6	60.00	25%	15.000	n/a			·	·	·	·	n/a			·	·	·	·			BLD-210	Only near full duty at the lowest bus voltage could it slow the build-up (BLD-225); not counted, as the force follows the measured current.	λ JUDGMENT OQ-010; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F02-022	R52, R56, R69, R70, R74, R75	100 kOhm 0402 gate-source pull-downs	Short: gate held at its source	FET cannot turn on: phase lost (FE-05)	RES-0402	6	1.80	10%	0.180	**Direct**	SM-31	60%	·	0.072	·	0.108	**Direct**	SM-31	90%	·	0.018	·	0.162			BLD-204	U5 VGS gate-fault monitor also flags it (OQ-007). RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-023	R52, R56, R69, R70, R74, R75	100 kOhm 0402 gate-source pull-downs	Open or drift	No SG-02 effect (gate undefined only while U5 is not driving: SG-01)	RES-0402	6	1.80	90%	1.620	n/a			·	·	·	·	n/a			·	·	·	·			BLD-218	Counted under SG-01 (F01-022).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-024	J7, J8, J9	Motor phase wire pads	Open (crack, lift) or short to an adjacent phase pad or the harness	Phase lost or windings shorted: no or too little torque (FE-05)	PAD	3	1.50	100%	1.500	**Direct**	SM-31	60%	·	**0.600**	·	0.900	**Direct**	SM-31	90%	·	**0.150**	·	1.350			BLD-212, BLD-213	An open phase leaves two-phase operation with low, rippled torque; a phase-to-phase short trips the shunt overcurrent. A rising joint resistance is not seen (BLD-213) but does not reduce the regulated current. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-025	Bus capacitors	C60, C73, C74, C61, C75, C76, C68	Short (hard or resistive) on 48V/12V_P	U1 short-circuit comparator or breaker removes the whole ECU supply: corner silent (FE-05, FE-07)	BUS-CAP		16.00	45%	7.200	**Direct**	SM-30	90%	·	**0.720**	·	6.480	**Direct**	SM-30	90%	·	**0.720**	·	6.480			BLD-401, BLD-402, BLD-403, PCB-201	TMO. A resistive short below the breaker level sags the bus and slows the build-up instead (FE-06); SM-31's apply-time check sees that only once BLD-225 sets the budget, so the resistive part is carried in the SM-30 miss. Split: 50 % of the MLCC, 30 % of the aluminium λ.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-022
F02-026	Bus capacitors	C60, C73, C74, C61, C75, C76, C68	Open, capacitance loss or ESR rise	No SG-02 effect (ripple and heating; SG-07)	BUS-CAP		16.00	55%	8.800	n/a			·	·	·	·	n/a			·	·	·	·			BLD-404, BLD-407		λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-030	R61, R80, R81	0.5 mOhm shunt BVN-Z	Resistance drift (one phase reads wrong)	Reading high: force below request (FE-05)	SHUNT	3	3.00	70%	2.100	**Direct**	SM-12	60%	·	**0.840**	·	1.260	**Direct**	SM-12	80%	·	**0.420**	·	1.680			BLD-306	As F01-030 (both drift directions counted, as SG-01 does). Sum check. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F02-031	R61, R80, R81	0.5 mOhm shunt BVN-Z	Open	Low-side conduction of one phase lost: drive stops or runs on two phases (FE-05)	SHUNT	3	3.00	30%	0.900	**Direct**	SM-31	60%	·	**0.360**	·	0.540	**Direct**	SM-31	90%	·	0.090	·	0.810			BLD-305	Safe for SG-01 (F01-031); here the lost phase is the violation. U5 Rsense and the CMPSS may trip first (OQ-007). RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-032	CSA front end	R60, R63, R78, R79, R82, R83, R71, R76, R77, C66, C70, C71, C78-C82, C84-C87	Open, short or drift of a Kelvin, filter or SOx part: one phase reads high, offset, frozen or noisy	Force below request (FE-05)	CSA-FE		8.20	70%	5.740	**Direct**	SM-12	60%	·	**2.296**	·	3.444	**Direct**	SM-12	80%	·	**1.148**	·	4.592			BLD-301 to BLD-304, BLD-307, BLD-309, BLD-318	As F01-032. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F02-033	CSA front end	R60, R63, R78, R79, R82, R83, R71, R76, R77, C66, C70, C71, C78-C82, C84-C87	Faults without a reading error	No SG-02 effect	CSA-FE		8.20	30%	2.460	n/a			·	·	·	·	n/a			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-034	R18, R132	7.5 kOhm IMON, 1 kOhm DC_BUS 0402	Open: IMON or DC_BUS pin driven above VDDA, ADC-A reference disturbed	Phase-current and angle readings on the same ADC wrong (FE-05)	RES-0402	2	0.60	60%	0.360	**Direct**	SM-12	60%	·	**0.144**	·	0.216	**Direct**	SM-12	80%	·	0.072	·	0.288			SUP-322, SUP-413	As F01-034. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F02-035	R18, R132	7.5 kOhm IMON, 1 kOhm DC_BUS 0402	Short or drift	No SG-02 effect (monitoring reading low)	RES-0402	2	0.60	40%	0.240	n/a			·	·	·	·	n/a			·	·	·	·			SUP-411		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-036	ADC reference network	L7, L8, L10, C44, C49, C83, C116, C117, C134	Ferrite open or capacitor short: VREFHI or VDDA of one ADC group lost	All readings of that group wrong: torque not as commanded (FE-05)	ADCREF-FE		5.40	50%	2.700	**Direct**	SM-12	60%	·	**1.080**	·	1.620	**Direct**	SM-12	80%	·	**0.540**	·	2.160			MCU-109, MCU-111, MCU-113, BLD-518	As F01-036. A C44/C83/C134 short also loads LDO3 (the U3 row F02-082 covers the monitor). RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F02-037	ADC reference network	L7, L8, L10, C44, C49, C83, C116, C117, C134	Capacitor open or capacitance loss, ferrite degraded	No SG-02 effect	ADCREF-FE		5.40	50%	2.700	n/a			·	·	·	·	n/a			·	·	·	·			MCU-115, PMC-209		λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-038	R39	0 Ohm 0402 (LDO3 to 3.3Vref)	Open	3.3Vref lost at U5 VREF and the ADC references while U14 runs (FE-05)	RES-0R		0.10	100%	0.100	**Direct**	SM-12	60%	·	0.040	·	0.060	**Direct**	SM-12	80%	·	0.020	·	0.080			PMC-202	The LDO3 monitor senses the U3 pin and does not see it (PMC-202); all readings go to a rail and fail the range check. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F02-040	U12	TMAG6180-Q1	SIN/COS wrong in range (offset, gain, phase), quadrant outputs wrong, or output stuck at a rail	Commutation angle wrong: torque reduced or reversed (FE-05)	U12-U13		10.00	65%	6.500	**Direct**	SM-14	90%	·	**0.650**	·	5.850	**Direct**	SM-14	97%	·	**0.195**	·	6.305			ANG-102, ANG-103, ANG-104, ANG-107,	F01-040 plus F01-041. An angle error of d gives torque of about cos(d) of the command. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-041	U12	TMAG6180-Q1	Internal diagnostic puts U12 in its safe state: outputs Hi-Z and held in range on C110/C111	Angle frozen: commutation stalls (FE-05)	U12-U13		10.00	20%	2.000	**Direct**	SM-14	90%	·	**0.200**	·	1.800	**Direct**	SM-14	97%	·	0.060	·	1.940			ANG-101, ANG-119, ANG-305	As built seen by the channel compare once the rotor moves; a rotor that does not move is also SM-31's no-motion case. With the actions the ANG-101 pull-downs take the node out of range. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-042	U12	TMAG6180-Q1	Faults without an output error	No SG-02 effect	U12-U13		10.00	15%	1.500	n/a			·	·	·	·	n/a			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F02-043	U13	TMAG6180-Q1	Output wrong in range, stuck, frozen (Hi-Z) or quadrant wrong	Monitor channel of the angle compare lost (latent)	U12-U13		10.00	85%	8.500	Latent	LM-12	90%	·	·	0.850	7.650	Latent	LM-12	97%	·	·	0.255	8.245	F02-040, F02-041, F02-050	11.09	ANG-201 to ANG-213	As F01-044. A detected U13 fault trips the compare and the corner reports itself: the safe state, not a violation.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-044	U13	TMAG6180-Q1	Faults without an output error	No SG-02 effect	U12-U13		10.00	15%	1.500	n/a			·	·	·	·	n/a			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F02-050	Angle front end ch1	R119, R121, R120, R122, C109, C110, C111, J21	Open, short or drift on SIN_P1/COS_P1, Q01/Q11 or the U12 supply pin	Channel-1 angle wrong or frozen: torque reduced (FE-05)	ANG-FE		3.70	70%	2.590	**Direct**	SM-14	90%	·	**0.259**	·	2.331	**Direct**	SM-14	97%	·	0.078	·	2.512			ANG-103, ANG-107 to ANG-111, ANG-114,	As F01-050. A C109 short pulls the 3.3 V rail down (ANG-114): TMO through the rail rows. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F02-051	Angle front end ch1	R119, R121, R120, R122, C109, C110, C111, J21	Faults within the error budget	No SG-02 effect	ANG-FE		3.70	30%	1.110	n/a			·	·	·	·	n/a			·	·	·	·			ANG-112	The uncompensated filter lag of ANG-112 is systematic, not counted here.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-052	Angle front end ch2	R123, R125, R124, R126, C112, C113, C114, J22	Open, short or drift on SIN_P2/COS_P2, Q02/Q12 or the U13 supply pin	Monitor channel of the angle compare lost (latent)	ANG-FE		3.70	70%	2.590	Latent	LM-12	90%	·	·	0.259	2.331	Latent	LM-12	97%	·	·	0.078	2.512	F02-040, F02-041, F02-050	11.09	ANG-204 to ANG-212	As F01-052.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F02-053	Angle front end ch2	R123, R125, R124, R126, C112, C113, C114, J22	Faults within the error budget	No SG-02 effect	ANG-FE		3.70	30%	1.110	n/a			·	·	·	·	n/a			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-060	U14	F29P329SM-Q1	CPU, memory or bus fault produces a wrong, low or frozen torque command	Too little or no torque at this wheel (FE-05)	U14		150.00	25%	37.500	**Direct**	SM-32	89%	·	**4.125**	·	33.375	**Direct**	SM-32	89%	·	**4.088**	·	33.413			BLD-101, MCU-503, MCU-514	Same mode and share as F01-060. The lockstep error resets U14, so the corner goes silent and is reported only by the status timeout: TMO, credited as SM-32 (SM-01 then SM-30).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F02-061	U14	F29P329SM-Q1	Fault common to both lockstep cores (internal clock, core supply, reset logic) that upsets program flow	Wrong or frozen command (FE-05)	U14		150.00	2%	3.000	**Direct**	SM-33	81%	·	**0.570**	·	2.430	**Direct**	SM-33	81%	·	**0.570**	·	2.430			MCU-507, MCU-112	As F01-061. The Q&A watchdog resets U14; TMO (SM-33 = SM-02 then SM-30). A frozen U14 that stops its status frames is seen by the timeout even without the watchdog.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-002
F02-062	U14	F29P329SM-Q1	BLDC PWM output pins (U14.88-93) stuck or shorted, or DRVOFF (U14.87) or nSLEEP (U14.86) stuck in the disable state	One phase or the whole bridge not driven (FE-05)	U14		150.00	2%	3.000	**Direct**	SM-31	60%	·	**1.200**	·	1.800	**Direct**	SM-31	90%	·	**0.300**	·	2.700			BLD-104, BLD-106, BLD-110, MCU-401, MCU-403,	F01-062 (0.015) plus the disable-state half of the DRVOFF/nSLEEP pin mode (0.005, taken from the SG-01 'other' share). The CPU keeps running, so SM-32 and SM-33 do not see it. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-063	U14	F29P329SM-Q1	ADC channel, multiplexer or sample-and-hold fault on a phase-current input	Reading high: force below request (FE-05)	U14		150.00	2%	2.250	**Direct**	SM-12	60%	·	**0.900**	·	1.350	**Direct**	SM-12	80%	·	**0.450**	·	1.800			MCU-111, MCU-307	As F01-064. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-064	U14	F29P329SM-Q1	ADC channel fault on one angle input	Commutation angle wrong: torque reduced (FE-05)	U14		150.00	1%	1.500	**Direct**	SM-14	90%	·	**0.150**	·	1.350	**Direct**	SM-14	97%	·	0.045	·	1.455			MCU-308, MCU-309	As F01-065. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038

Failure modes											VerB as built								With DFMEA actions								Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)		Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected		Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected		Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F02-065	U14	F29P329SM-Q1	ADC module or reference fault common to both angle channels (both converted on one module)	Same angle error on both channels: the compare agrees, torque reduced (FE-05)	U14		150.00	1%	1.500		**Direct**			**1.500**	·	·	·		**Direct**	**SM-15**	80%	·	**0.300**	·	1.200			ANG-306, MCU-118	As F01-066: no detection as built. RPT with the actions.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-066	U14	F29P329SM-Q1	MCAN peripheral or message-RAM fault delivers a wrong, stale or lost clamp-force request	Force below request, or request ignored (FE-05, FE-06)	U14		150.00	1%	1.500		**Direct**	SM-16	90%	·	**0.150**	·	1.350		**Direct**	SM-16	90%	·	**0.150**	·	1.350			MCU-508, CAN-102, CAN-131	As F01-067. The E2E failure releases the corner and reports it unavailable (RPT); a request that is valid but low for this corner is a brake-controller fault, not counted here.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-040
F02-067	U14	F29P329SM-Q1	Status transmit path (MCAN TX, message RAM) or flash/boot fault: status frames lost, frozen, or U14 does not start	Corner lost or not started without a report (FE-07)	U14		150.00	1%	1.500		**Direct**	SM-30	90%	·	**0.150**	·	1.350		**Direct**	SM-30	90%	·	**0.150**	·	1.350			MCU-509, MCU-205, MCU-206, MCU-605	Frozen frames fail the alive counter; lost frames and a U14 stuck in a boot loader fail the timeout. TMO.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-022
F02-068	U14	F29P329SM-Q1	SPI peripheral to U5 writes wrong data or corrupts readback	U5 configuration wrong: drive weakened or stopped (FE-05)	U14		150.00	1%	0.750		**Direct**	SM-13	80%	·	**0.150**	·	0.600		**Direct**	SM-13	80%	·	**0.150**	·	0.600			BLD-113, BLD-115	The lockstep does not cover the peripheral; the readback does. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-069	U14	F29P329SM-Q1	Lockstep comparator, ECC or error-signal module fault	MCU self-monitoring blind (latent)	U14		150.00	5%	7.500		Latent	LM-04	90%	·	·	0.750	6.750		Latent	LM-04	90%	·	·	0.750	6.750		F02-060	37.50	MCU-504, MCU-505, MCU-506	As F01-068.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F02-070	U14	F29P329SM-Q1	Other MCU functions (EPB, wheel speed, pedal capture, other peripherals); DRVOFF or nSLEEP pin stuck in the enable state	Not counted for SG-02	U14		150.00	60%	90.000		n/a			·	·	·	·		n/a			·	·	·	·					F01-069 (0.615) less the 0.005 of F02-062 and the 0.01 of F02-067 and 0.005 of F02-068, plus F01-063 (0.005, SG-01 only).	λ GATED OQ-007; share JUDGMENT
F02-080	U3	TPS653860-Q1	Watchdog or error monitor fails to act, or NRST cannot reset the MCU	Reset reaction for MCU and rail faults lost (latent)	U3		40.00	8%	3.200		Latent	LM-05	90%	·	·	0.320	2.880		Latent	LM-05	90%	·	·	0.320	2.880		F02-061, F02-082, F02-100, F02-103	11.84	PMC-402, PMC-404, PMC-405	As F01-070. Partners: the rows whose detection ends in an NRST (SM-33, SM-34).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F02-081	U3	TPS653860-Q1	SAFE_OUT1 asserts without a fault	U5 put to sleep: no torque (FE-05)	U3		40.00	2%	0.600		n/a			·	·	·	·		**Direct**	**SM-31**	90%	·	0.060	·	0.540			PMC-401, BLD-120	SAFE_OUT1 is unconnected on VerB. With the actions it drives U5 nSLEEP (BLD-120), so a spurious assertion stops the drive while U14 runs. Half of the 0.03 SAFE_OUT1 share of F01-071; the fail-to-assert half is in F02-092. RPT.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-082	U3	TPS653860-Q1	LDO1 (3.3 V), LDO3 (3.3Vref), LDO2 (5 V) or the buck-boost regulates outside its monitor window, high or low	U14, U5, the sensors or the CAN transceivers browned out or overdriven: drive and readings lost (FE-05)	U3		40.00	11%	4.400		**Direct**	SM-34	81%	·	**0.836**	·	3.564		**Direct**	SM-34	81%	·	**0.836**	·	3.564			PMC-105, PMC-114, PMC-203, PMC-206, ANG-305, CAN-111	F01-072 (0.07) plus buck-boost high (0.03) and LDO2 high (0.01, as F05-080). The monitor resets U14: TMO. LDO1 low between 2.3 and 2.65 V freezes both angle channels unless the UV threshold is above 2.65 V (ANG-305, OQ-002).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F02-083	U3	TPS653860-Q1	LDO1 or LDO3 drifts inside the monitor window	Same angle offset on both channels, phase currents scaled: force below request (FE-05)	U3		40.00	4%	1.600		**Direct**			**1.600**	·	·	·		**Direct**	**SM-15**	80%	·	**0.320**	·	1.280			PMC-201, ANG-113, MCU-302	As F01-073: no detection as built. RPT with the actions.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F02-084	U3	TPS653860-Q1	Rail monitors (EXT_VMON1, LDO1, LDO2, LDO3, BB_OUT) stuck at 'good'	Supply faults no longer detected (latent)	U3		40.00	3%	1.200		Latent	LM-05	90%	·	·	0.120	1.080		Latent	LM-05	90%	·	·	0.120	1.080		F02-082, F02-100, F02-103	8.84	PMC-214, PMC-312, PMC-317	As F01-074. A rail that collapses silences the corner without its monitor, so the SM-30 rows are not partners.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F02-085	U3	TPS653860-Q1	Spurious reset or safe state (NRST asserted, U14 held in reset or cycling)	Corner stops braking and goes silent (FE-05, FE-07)	U3		40.00	10%	4.000		**Direct**	SM-30	90%	·	**0.400**	·	3.600		**Direct**	SM-30	90%	·	**0.400**	·	3.600			PMC-407, PMC-408, PMC-410, PMC-311	Safe for SG-01 (F01-075); for SG-02 this is the silent loss HE-12 describes. U3 cannot report it (U14 is its only reader, PMC-408). TMO. A reset loop shorter than the timeout is closed only by PMC-419's reset-cause rule (scenario B).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-022
F02-086	U3	TPS653860-Q1	Buck-boost (VCC_6V0) lost; LDO1, LDO2 or LDO3 output lost (current limit, thermal or internal-supply shutdown); SPI or internal supply lost	All logic rails or both CAN channels lost: corner silent (FE-05, FE-07)	U3		40.00	37%	14.800		**Direct**	SM-30	90%	·	**1.480**	·	13.320		**Direct**	SM-30	90%	·	**1.480**	·	13.320			PMC-107, PMC-109, PMC-110, PMC-113, PMC-118,	Split from F01-076 (0.65 n/a for SG-01): buck-boost 0.20, LDO1/LDO3 0.10, LDO2 0.04, internal supply, overtemperature and SPI 0.03. TMO (PMC-118).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-022
F02-092	U3	TPS653860-Q1	Other PMIC functions (PLDO1/2 pedal supplies, EPB-related, LDO4, LDO2 low in a band where only U6 is affected); SAFE_OUT1 fails to assert	Not counted for SG-02	U3		40.00	26%	10.200		n/a			·	·	·	·		n/a			·	·	·	·					Rest of F01-076 plus the fail-to-assert half of F01-071.	λ GATED OQ-007; share JUDGMENT
F02-100	U4	TPS62902-Q1	1.25 V core regulated high or low (TI 'output out of specification'), or high-side FET stuck on	U14 core overdriven or browned out: erratic or no command (FE-05)	U4		12.00	32%	3.840		**Direct**	SM-34	81%	·	**0.730**	·	3.110		**Direct**	SM-34	81%	·	**0.730**	·	3.110			PMC-301, PMC-303, PMC-304, PMC-307, PMC-315	F01-080 and F01-081 (0.21) plus the low half of TI's out-of-spec mode (0.11). EXT_VMON1 resets U14: TMO. The HS short may damage U14 before the monitor acts (PMC-304); the corner is then silent all the same.	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F02-101	U4	TPS62902-Q1	Output lost: low-side FET stuck on, power-FET damage, enable fault	U14 core lost: corner silent (FE-05, FE-07)	U4		12.00	55%	6.600		**Direct**	SM-30	90%	·	**0.660**	·	5.940		**Direct**	SM-30	90%	·	**0.660**	·	5.940			PMC-306, PMC-308	TI SFFS465A: LS half of 'HS or LS stuck on' 10 %, FET damage 36 %, EN 9 %. VDD POR holds U14 in reset. TMO.	λ JUDGMENT OQ-010; DC PROVISIONAL OQ-022
F02-102	U4	TPS62902-Q1	Power-good output faults	No SG-02 effect (the rail itself is unaffected)	U4		12.00	13%	1.560		n/a			·	·	·	·		n/a			·	·	·	·					TI SFFS465A 13 %.	λ JUDGMENT OQ-010
F02-103	R46, R48	107 kOhm, 100 kOhm 0402 (U4 feedback)	Open, short or drift: core regulated high, low or at 0 V	U14 core overdriven or browned out (FE-05)	RES-0402	2	0.60	100%	0.600		**Direct**	SM-34	81%	·	**0.114**	·	0.486		**Direct**	SM-34	81%	·	**0.114**	·	0.486			PMC-301, PMC-316	F01-083 and F01-084 together: both directions are SG-02 faults. EXT_VMON1 has its own divider. Drift within tolerance is carried here rather than split out. TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-002
F02-104	R44, R47	16.2 kOhm, 15 kOhm 0402 (EXT_VMON1 divider)	Drift: core monitor threshold shifted	Core fault detected late or not at all (latent)	RES-0402	2	0.60	30%	0.180		Latent			·	·	0.180	·		Latent			·	·	0.180	·	F02-100, F02-103	4.44	PMC-312, PMC-314	As F01-085; no test of the divider exists.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-105	R44, R47	16.2 kOhm, 15 kOhm 0402 (EXT_VMON1 divider)	Open or short	Spurious UV or OV trip holds U14 in reset: corner silent (FE-05, FE-07)	RES-0402	2	0.60	70%	0.420		**Direct**	SM-30	90%	·	0.042	·	0.378		**Direct**	SM-30	90%	·	0.042	·	0.378			PMC-311, PMC-408	Safe for SG-01 (F01-086); a false trip is the SG-02 violation until the timeout reports it. TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-022
F02-110	R134, R136	1 kOhm, 10 kOhm 0402 (ERRORSTS)	Open, short or drift: GPI1 held at the no-error level, floating, or not driven by U14	PMIC escalation of U14 errors lost (latent)	RES-0402	2	0.60	100%	0.600		Latent	LM-05	90%	·	·	0.060	0.540		Latent	LM-05	90%	·	·	0.060	0.540		F02-061	3.00	PMC-409, MCU-515	F01-090 (open, 0.60) plus F01-091 (0.40) counted latent as a whole: R136 holds MCU_ERRORSTS at the no-error level, so its short also blinds the escalation, and R134 short or drift has no effect. Conservative; not split further.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F02-120	U2	LM68645-Q1	Output lost or below the CMPSS undervoltage level; high-side FET short (12 V pulled toward 48V/12V_P)	PMIC input or the whole ECU supply removed: corner silent (FE-05, FE-07)	U2		20.00	95%	19.000		**Direct**	SM-30	90%	·	**1.900**	·	17.100		**Direct**	SM-30	90%	·	**1.900**	·	17.100			BCK-102, BCK-104, BCK-106, BCK-203, PMC-117, BCK-101	Lost or low: U3 loses its input, or the CMPSS 10.8 V window drops INH. HS short: the SM-09 cut-off removes 48V/12V_P (as F01-100); if it fails, the overvoltage damages U3 and U5 and the corner goes silent anyway. TMO. F01-100 (0.10) plus F01-101 less the band of F02-121.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-022
F02-121	U2	LM68645-Q1	12 V output low in a band where U3 and U14 run but U5 GVDD is below its requirement	Gate drive weak or off while U14 still reports available (FE-05)	U2		20.00	5%	1.000		**Direct**	SM-31	60%	·	**0.400**	·	0.600		**Direct**	SM-31	90%	·	**0.100**	·	0.900			BLD-504, BLD-524, BCK-207	Same 0.05 as F05-093. U5 GVDD UV sends nFAULT; SM-31 sees the drive fail. RPT. The CMPSS UV window may also cut the corner off (then TMO).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F02-122	R33, R35	100 kOhm, 7.15 kOhm 0402 (U2 feedback)	Open, short or drift: 12 V driven toward the input or regulated low	SM-09 cut-off or U3 input loss: corner silent (FE-05, FE-07)	RES-0402	2	0.60	100%	0.600		**Direct**	SM-30	90%	·	0.060	·	0.540		**Direct**	SM-30	90%	·	0.060	·	0.540			BCK-201, BCK-202, BCK-203	F01-102 and F01-103 together; both directions end in a silent corner. TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-022
F02-123	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Open or short	CMPSS window trips on a good 12 V rail: corner cut off (FE-05, FE-07)	RES-0402	2	0.60	70%	0.420		**Direct**	SM-30	90%	·	0.042	·	0.378		**Direct**	SM-30	90%	·	0.042	·	0.378			MCU-305, SUP-323	Safe for SG-01 (F01-105); here the false cut-off is the violation until the timeout reports it. TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-022
F02-124	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Drift within the window	No SG-02 effect (the overvoltage cut-off is not an SG-02 mechanism)	RES-0402	2	0.60	30%	0.180		n/a			·	·	·	·		n/a			·	·	·	·					Latent for SG-01 (F01-104).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F02-130	U1	LM74930-Q1	IMON fault (TI 5 %): IMON drives U14.35 above the ADC range	ADC-A reference disturbed: phase-current and angle readings wrong (FE-05)	U1		14.00	5%	0.700	**Direct**	SM-12	60%	·	**0.280**	·	0.420	**Direct**	SM-12	80%	·	**0.140**	·	0.560			SUP-321, SUP-322	As F01-111. RPT.	DC PROVISIONAL OQ-038
F02-131	U1	LM74930-Q1	HGATE out of spec or stuck low (TI 26 %); false OCP, SCP, UV or OV trip; pin short that switches Q1 off	48V/12V_P lost: corner silent (FE-05, FE-07)	U1		14.00	50%	7.000	**Direct**	SM-30	90%	·	**0.700**	·	6.300	**Direct**	SM-30	90%	·	**0.700**	·	6.300			SUP-212, SUP-221, SUP-307, SUP-312, SUP-315,	Half of TI's OCP, SCP, UV/OV and pin-short modes is taken as a false trip, half as a lost protection (F02-132): sev10 judgment. nFLT_LM74930 asserts but U14 loses supply with it. TMO.	share JUDGMENT; DC PROVISIONAL OQ-022
F02-132	U1	LM74930-Q1	DGATE modes (TI 40 %), HGATE stuck high (5 %), lost OCP/SCP/UV/OV protection	No SG-02 effect (Q2 body diode carries the load; protections against external events lost)	U1		14.00	45%	6.300	n/a			·	·	·	·	n/a			·	·	·	·			SUP-218, SUP-311, SUP-314	HGATE stuck high is latent for SG-01 and SG-03 (SM-09); SM-09 is not an SG-02 mechanism.	share JUDGMENT
F02-133	Q1, Q2	SQJA90EP	Q1 drain-source open or gate-source short; Q2 drain-source open	48V/12V_P lost: corner silent (FE-05, FE-07)	FET-80V	2	20.00	28%	5.500	**Direct**	SM-30	90%	·	**0.550**	·	4.950	**Direct**	SM-30	90%	·	**0.550**	·	4.950			SUP-212, SUP-213, SUP-214,	(Q1 0.20 + 0.15 + Q2 0.20) / 2. TMO.	λ JUDGMENT OQ-010; share JUDGMENT; DC PROVISIONAL OQ-022
F02-134	Q1, Q2	SQJA90EP	Q1 short or on-resistance increase; Q2 short, gate-source short or on-resistance increase	No SG-02 effect (Q2 body diode carries the load; reverse or overvoltage protection lost)	FET-80V	2	20.00	73%	14.500	n/a			·	·	·	·	n/a			·	·	·	·			SUP-218, SUP-219	The Q1 short is latent for SG-01 (F01-113).	λ JUDGMENT OQ-010; share JUDGMENT
F02-135	INH network	D6, D7, R102, R112, R156, R19, R26, R36	INH_CAN pulled or held low (diode open in the only active path, series resistor open, node shorted to GND)	U1 and U2 disabled: corner off (FE-05, FE-07)	INH-NET		3.80	30%	1.140	**Direct**	SM-30	90%	·	**0.114**	·	1.026	**Direct**	SM-30	90%	·	**0.114**	·	1.026			CAN-410, SUP-401	TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-022
F02-136	INH network	D6, D7, R102, R112, R156, R19, R26, R36	One transceiver's INH contribution lost (the other holds INH_CAN); R156 open	No SG-02 effect	INH-NET		3.80	70%	2.660	n/a			·	·	·	·	n/a			·	·	·	·			CAN-406, CAN-409	R156 open is latent for SG-01 (F01-117).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-137	J3, J4	Supply wire pads	Open, intermittent, or short to an adjacent pad or the harness	ECU supply lost or interrupted: corner silent (FE-05, FE-07)	PAD	2	1.00	100%	1.000	**Direct**	SM-30	90%	·	**0.100**	·	0.900	**Direct**	SM-30	90%	·	**0.100**	·	0.900			SUP-113, PCB-501	A short to ground also opens the vehicle fuse of the domain (MC-01, dependent-failure note). TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-022
F02-138	Supply passives	D1, D3, D11, R99, C5-C10, C12, C16, C21-C24, C28, L1-L4, R7, Q3, Q12, U1/U2 support networks, PMIC and rail links	Series part open (inductor, shunt, link, Q3), shunt drifting high, capacitor or TVS short, VSUP dropper open, U1/U2 divider fault that trips or disables the supply	48V/12V_P, 12V, VSUP or a logic rail lost: corner silent (FE-05, FE-07)	PWR-PASS		45.00	44%	19.800	**Direct**	SM-30	90%	·	**1.980**	·	17.820	**Direct**	SM-30	90%	·	**1.980**	·	17.820			SUP-111, SUP-117, SUP-118, SUP-303, SUP-308, SUP-324, BCK-111,	Share from the class split of each part (see the proposed FIT entry). TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-022
F02-139	Supply passives	D1, D3, D11, R99, C5-C10, C12, C16, C21-C24, C28, L1-L4, R7, Q3, Q12, U1/U2 support networks, PMIC and rail links	Capacitor open or capacitance loss, TVS open, shunt drifting low, Q3 short, divider drift inside its window	No SG-02 effect (filtering or a protection against external events lost)	PWR-PASS		45.00	56%	25.200	n/a			·	·	·	·	n/a			·	·	·	·			SUP-105, SUP-225, SUP-418	Latent losses of external-event protections are not random-fault mechanisms (as F05-016).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F02-140	Rail decoupling	1.25V: C57, C58, C123-C132; 3.3V: C37, C43, C48, C91, C98, C103, C107, C121, C122, C137-C147; 5V: C46, C51, C92, C101, C105; 12V: C27, C31-C36, C89; 12V_Cobra: C25, C26, C30; VCC_6V0: C40, C41, C42, C56	Short (crack, dielectric breakdown, pad bridge)	Rail collapses: U14, U5 and both CAN channels lost together, corner silent (FE-05, FE-07)	RAIL-DEC		31.30	50%	15.650	**Direct**	SM-30	90%	·	**1.565**	·	14.085	**Direct**	SM-30	90%	·	**1.565**	·	14.085			PMC-103, PMC-104, PMC-111, MCU-104, MCU-106, CAN-112, CAN-113, CAN-213, CAN-214, BCK-403, BLD-515, WSS-104,	The rows SG-01 and SG-05 leave out. A resistive short that only sags the rail meets the PMIC UV monitor first (reset, then the same timeout). TMO.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-022
F02-141	Rail decoupling	1.25V: C57, C58, C123-C132; 3.3V: C37, C43, C48, C91, C98, C103, C107, C121, C122, C137-C147; 5V: C46, C51, C92, C101, C105; 12V: C27, C31-C36, C89; 12V_Cobra: C25, C26, C30; VCC_6V0: C40, C41, C42, C56	Open or capacitance loss	No SG-02 effect (each rail has several capacitors in parallel)	RAIL-DEC		31.30	50%	15.650	n/a			·	·	·	·	n/a			·	·	·	·			MCU-107, PMC-105, PMC-316	Loss of the only bulk of a regulator output (C48, C57) can make it oscillate; that shows as ripple outside the monitor window and is carried by F02-082 and F02-100.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-150	Y1	CDC6C-Q1	No output clock, or wrong frequency	U14 timebase lost or wrong: control loop, PWM and CAN timing wrong (FE-05, FE-06)	Y1		3.00	60%	1.800	**Direct**	SM-21	90%	·	**0.180**	·	1.620	**Direct**	SM-21	90%	·	**0.180**	·	1.620			MCU-201, MCU-202, MCU-203, MCU-209	TI SFFS685: no clock 30 %, wrong frequency 30 %. U14 runs on INTOSC after the missing-clock detection and the DCC flags a wrong frequency, so U14 can still report (RPT), provided SM-21's reaction also reports the corner (see the proposed notes).	DC GATED OQ-007
F02-151	Y1	CDC6C-Q1	Clock degraded (jitter, duty cycle) within the PLL range	No SG-02 effect	Y1		3.00	40%	1.200	n/a			·	·	·	·	n/a			·	·	·	·			MCU-202	TI SFFS685 40 %.	
F02-152	R137	33 Ohm 0402 (X1 series)	Open	Clock lost at X1 (FE-05)	RES-0402		0.30	60%	0.180	**Direct**	SM-21	90%	·	0.018	·	0.162	**Direct**	SM-21	90%	·	0.018	·	0.162			MCU-202	As F05-073. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F02-153	R137	33 Ohm 0402 (X1 series)	Short or drift	No SG-02 effect	RES-0402		0.30	40%	0.120	n/a			·	·	·	·	n/a			·	·	·	·			MCU-202		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-160	U8, U10	TCAN1043H-Q1	Receiver or transmitter fail, stuck in sleep, bus dominant (TI 35 + 35 + 15 + 5 %)	One CAN channel lost: request and status continue on the other; both lost: the corner is silent and the timeout reports it	TCAN	2	18.00	90%	16.200	Safe			·	·	·	·	Safe			·	·	·	·			CAN-105, CAN-107, CAN-108, CAN-114, CAN-201, CAN-221	Safe, not latent: no single transceiver fault loses braking, and the loss of both is itself caught by SM-30, so a violation needs a third fault (outside this ECU). Assumes the request and status are sent on both channels (OQ-039). A dominant bus blocks that channel for the other nodes too (MC-01, dependent-failure note).	share JUDGMENT
F02-161	U8, U10	TCAN1043H-Q1	Pin-to-pin short (TI 5 %): VCC, VIO or INH shorted	Shared 5 V or 3.3 V pulled down, or INH released: corner silent (FE-05, FE-07)	TCAN	2	18.00	5%	0.900	**Direct**	SM-30	90%	·	0.090	·	0.810	**Direct**	SM-30	90%	·	0.090	·	0.810			CAN-111, CAN-112, CAN-113, CAN-407	Counted whole for SG-02 (SG-01 takes 0.02 of it for the INH case). TMO.	share JUDGMENT; DC PROVISIONAL OQ-022
F02-162	U8, U10	TCAN1043H-Q1	False fault report (TI 5 %)	No SG-02 effect	TCAN	2	18.00	5%	0.900	n/a			·	·	·	·	n/a			·	·	·	·					
F02-170	New (BLD-102, BLD-120)	U5 input pulls (DRVOFF pull-up, nSLEEP pull-down, nCS pull-up, 6 PWM pull-downs) and the 1 kOhm nSLEEP series resistor	Pull resistor short (holds DRVOFF high, nSLEEP, a PWM input or nCS at the off level), or the nSLEEP series resistor open	Drive or one phase held off, or U5 unreachable: no or too little torque (FE-05)	RES-0402	10	3.00	15%	0.450	n/a			·	·	·	·	**Direct**	**SM-31**	90%	·	0.045	·	0.405			BLD-102, BLD-120	(9 × 10 % short + 60 % open of the series part) / 10. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-032
F02-171	New (BLD-102, BLD-120)	U5 input pulls (DRVOFF pull-up, nSLEEP pull-down, nCS pull-up, 6 PWM pull-downs) and the 1 kOhm nSLEEP series resistor	Pull resistor open or drift; series resistor short or drift	No SG-02 effect (SG-01: F01-150, F01-152)	RES-0402	10	3.00	85%	2.550	n/a			·	·	·	·	n/a			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F02-172	New (ANG-101)	100 kOhm SIN/COS pull-downs at U14	Open: a Hi-Z sensor output is held in range again	Fast detection of a sensor in its safe state lost (latent)	RES-0402	4	1.20	60%	0.720	n/a			·	·	·	·	**Latent**			·	·	0.720	·	F02-041	2.00	ANG-101, ANG-201	As F01-154; nothing tests the pull-down itself.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F02-173	New (ANG-101)	100 kOhm SIN/COS pull-downs at U14	Short or drift	Short: angle input at 0 V, commutation lost (FE-05)	RES-0402	4	1.20	40%	0.480	n/a			·	·	·	·	**Direct**	**SM-14**	97%	·	0.014	·	0.466			ANG-101	The range check flags a 0 V input within one sample; drift of a 100 kOhm pull-down is carried here rather than split out. RPT.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F02-174	New (BLD-201)	Phase isolation FETs (back-to-back, two phases)	Drain-source open or gate-source short	Phase disconnected: no or too little torque (FE-05)	FET-80V	4	40.00	35%	14.000	n/a			·	·	·	·	**Direct**	**SM-31**	90%	·	**1.400**	·	12.600			BLD-201	The isolation adds series parts whose opening is an SG-02 fault (F01-157 is Safe for SG-01). A spurious opening by its driver is part of this row. RPT.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F02-175	New (BLD-201)	Phase isolation FETs (back-to-back, two phases)	Drain-source short or on-resistance increase	No SG-02 effect (isolation cannot open: SG-01 latent, F01-156)	FET-80V	4	40.00	65%	26.000	n/a			·	·	·	·	n/a			·	·	·	·					λ JUDGMENT OQ-010; share JUDGMENT (class split)
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**309.41 λ**			**3.100**	**56.305**	**2.539**	**231.266**	**325.66 λ**			**0.000**	**31.185**	**2.483**	**275.792**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-03 · Computed (Rev A, provisional)

ASIL D

Avoid parking-brake application while the vehicle is moving, unless the driver requests it

Safe state: EPB actively released and further apply inhibited (de-energising alone keeps the force on a self-locking spindle)

FTTI: TBD; provisional 300 ms (ASSUMED) · Hazardous events: HE-13 (S10-QLN-HARA-001 Rev B)

	SPFM · target ≥ 99%	LFM · target ≥ 90%	PMHF (FIT) · item < 10 FIT; corner share open (OQ-046)
As built	96.70%	95.19%	3.99
With actions	98.65%	94.65%	1.63

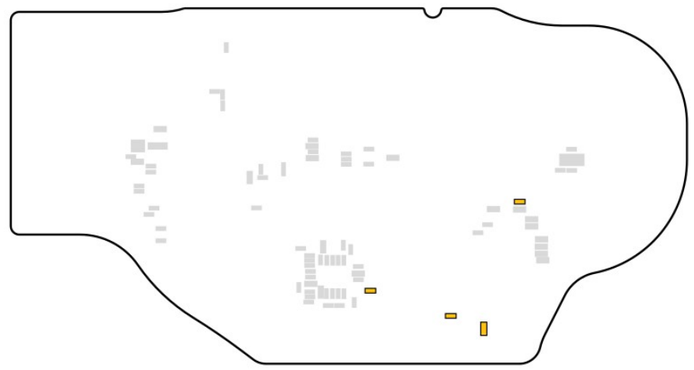
Key findings

1. As built, SG-03 has two single-point faults: a U7 output stage that drives the apply direction on its own (the only independent switch, the Q11 cut-off, cannot open because R58 ties its gate to the bus) and U14 EPB pins stuck in the drive state (the lockstep does not see a port fault and the only reaction runs through those pins). A U7 input fault is covered at Low only, because its reaction acts in the same die. Direction: R58 not fitted, OUTA/OUTB readback, SAFE_OUT1 to nSLEEP (EPB-211, EPB-401, EPB-408).
2. With the actions SG-03 still falls just short of its SPFM target on the ASSUMED data. The remaining gap is supply overvoltage on the MCU rails (U4 core, U3 LDO1, U2 12 V), credited at Medium until the PMIC monitor thresholds and reaction are known (OQ-002, OQ-014); High coverage there closes it. The cut-off reactions stop an apply without releasing it, so their credit holds only if they act before the force is hazardous (EPB-409, OQ-047).
3. The PMHF cannot be judged until the corner ECU's share of the item budget is set (OQ-046): with two EPB corners per vehicle, SG-03 alone takes about twice the value shown.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Elements that can apply the EPB or stop an unintended apply: the EPB driver and its parts (U7, Q11 cut-off and their passives, the wire pads J5/J6, the shared SPI-D resistors), the parts of the MCU (U14), PMIC (U3) and BLDC driver (U5) that command or stop the EPB, the supply rails whose overvoltage can corrupt the MCU (U4, U3 LDO1, U2) and the input stage U1, the MCU clock (Y1), the CAN path that carries the independent speed, and the standstill information (U6, its decoupling and its front end). Loss of a rail removes power from the EPB and is safe for SG-03. U14.84 (CUTOFF_ASCIN) acts only through Q6, which the actions remove; as built the cut-off serves no mechanism.

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F03-001	U7	DRV8263-Q1	Output stage drives the motor in the apply direction without a command (diagonal FET pair shorted or gate drive stuck on)	EPB applies while moving	U7		20.00	4%	0.800	**Direct**			**0.800**	·	·	·	**Direct**	**SM-04**	90%	·	0.080	·	0.720			EPB-211, EPB-314	As built no mechanism acts: DRVOFF is in the failed die, the IPROPI mirror is blind to a shorted high-side FET and Q11 cannot open (R58). Opening Q11 stops the apply but keeps the force built so far and removes the release path; the credit assumes the timing budget of EPB-409 (OQ-047).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-029
F03-002	U7	DRV8263-Q1	Output stage drives the release direction without a command	No SG-03 effect (hold lost: SG-04)	U7		20.00	4%	0.800	Safe			·	·	·	·	Safe			·	·	·	·			EPB-211		λ GATED OQ-007; share JUDGMENT
F03-003	U7	DRV8263-Q1	Input logic fault (EN/IN1 or PH/IN2 buffer, state machine) drives the bridge without a command	EPB applies while moving	U7		20.00	4%	0.800	**Direct**	SM-03	60%	·	**0.320**	·	0.480	**Direct**	SM-03	90%	·	0.080	·	0.720			EPB-103	DRVOFF faults are F03-004. As built the reaction (DRVOFF) acts in the same die as the fault, hence Low coverage; with the actions it opens Q11 (OQ-047 timing).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-004	U7	DRV8263-Q1	DRVOFF no longer disables the bridge	Stop path for MCU faults lost (latent)	U7		20.00	6%	1.200	Latent	LM-01	90%	·	·	0.120	1.080	Latent	LM-01	90%	·	·	0.120	1.080	F03-020, F03-021	31.50	EPB-102, EPB-105		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-005	U7	DRV8263-Q1	Current-sense output (IPROPI) wrong or zero	Unintended-motion monitor blind (latent)	U7		20.00	8%	1.600	Latent	LM-02	90%	·	·	0.160	1.440	Latent	LM-02	90%	·	·	0.160	1.440	F03-003, F03-021	2.30	EPB-319		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-006	U7	DRV8263-Q1	Register corruption unlocks SPI control and commands a drive (S_DRVOFF = 0, S_ENIN1 = 1)	EPB applies while moving	U7		20.00	4%	0.800	**Direct**	SM-05	90%	·	0.080	·	0.720	**Direct**	SM-05	90%	·	0.080	·	0.720			EPB-501, EPB-502		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-007	U7	DRV8263-Q1	Fault reporting (nFAULT, STATUS, SPI readback) lost or wrong	Diagnostics of U7 blind (latent)	U7		20.00	10%	2.000	Latent	LM-06	90%	·	·	0.200	1.800	Latent	LM-06	90%	·	·	0.200	1.800	F03-006, F03-022	2.30	EPB-507, EPB-509		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-008	U7	DRV8263-Q1	Outputs off or high impedance; the bridge cannot drive	No SG-03 effect (EPB unavailable: SG-04, SG-06)	U7		20.00	30%	6.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-209, EPB-212		λ GATED OQ-007; share JUDGMENT
F03-009	U7	DRV8263-Q1	VM or GND pin short, internal supply short	No SG-03 effect (supply collapses; thermal event: SG-07)	U7		20.00	5%	1.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-201		λ GATED OQ-007; share JUDGMENT
F03-012	U7	DRV8263-Q1	OUTA or OUTB pin shorted to VM or GND	A second fault (over-current protection lost) lets the short drive the motor (latent)	U7		20.00	5%	1.000	Latent	LM-07	60%	·	·	0.400	0.600	Latent	LM-07	60%	·	·	0.400	0.600	F03-010	1.00	EPB-203, EPB-205	At idle U7 is Hi-Z (DRVOFF high) or in brake with both low sides on (OQ-032). Hi-Z: no current path. Brake: the short runs through a low-side FET and the U7 over-current protection turns the bridge off within microseconds, so the short alone cannot drive the motor.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-010	U7	DRV8263-Q1	Over-current protection lost	An OUTx short then drives the motor (latent)	U7		20.00	5%	1.000	Latent			·	·	1.000	·	Latent			·	·	1.000	·	F03-012, F03-089	1.30	EPB-221	No test of the over-current protection exists, so the full λ counts as latent.	λ GATED OQ-007; share JUDGMENT
F03-013	U7	DRV8263-Q1	Thermal protection lost	No SG-03 effect (SG-07 latent)	U7		20.00	5%	1.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-214		λ GATED OQ-007; share JUDGMENT
F03-011	U7	DRV8263-Q1	Other internal faults (charge pump, oscillator, SPI timing) that stop the bridge	No SG-03 effect	U7		20.00	10%	2.000	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F03-020	U14	F29P329SM-Q1	CPU, memory or bus fault produces an erroneous EPB apply command	EPB applies while moving	U14		150.00	20%	30.000	**Direct**	SM-01	99%	·	**0.300**	·	29.700	**Direct**	SM-01	99%	·	**0.300**	·	29.700			EPB-101, MCU-503	Share of U14 that computes and issues the EPB command. The lockstep reaction resets U14 through the PMIC; the pins float and U7 turns off.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F03-021	U14	F29P329SM-Q1	EPB control pins (U14.2 DRVOFF, U14.11, U14.98) stuck in the drive state (port fault the lockstep does not see)	EPB applies while moving	U14		150.00	1%	1.500	**Direct**			**1.500**	·	·	·	**Direct**	**SM-03**	90%	·	**0.150**	·	1.350			EPB-101, EPB-408	The CPU keeps running and servicing the watchdog, so the watchdog does not see it (EPB-101). As built the current check can see it but can only react through the stuck pins. With the actions SM-03 opens Q11 and SAFE_OUT1 puts U7 to sleep, neither through U14's EPB pins.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-022	U14	F29P329SM-Q1	SPI-D peripheral fault writes wrong data to U7	EPB applies while moving	U14		150.00	1%	1.500	**Direct**	SM-05	90%	·	**0.150**	·	1.350	**Direct**	SM-05	90%	·	**0.150**	·	1.350			EPB-512, EPB-517		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-023	U14	F29P329SM-Q1	Lockstep comparator, ECC or error-signal module fault	MCU self-monitoring blind (latent)	U14		150.00	5%	7.500	Latent	LM-04	90%	·	·	0.750	6.750	Latent	LM-04	90%	·	·	0.750	6.750	F03-020	30.00	MCU-504, MCU-505, MCU-506		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F03-024	U14	F29P329SM-Q1	Isense_EPB ADC channel reads wrong	Unintended-motion monitor blind (latent)	U14		150.00	1%	1.500	Latent	LM-02	90%	·	·	0.150	1.350	Latent	LM-02	90%	·	·	0.150	1.350	F03-003, F03-021	2.30	EPB-302		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F03-026	U14	F29P329SM-Q1	CAN receive path (MCAN, message RAM) delivers a wrong vehicle speed	Independent standstill source corrupted (latent: a false standstill from U6 is then accepted)	U14		150.00	1%	1.500	Latent	LM-08	90%	·	·	0.150	1.350	Latent	LM-08	90%	·	·	0.150	1.350	F03-100, F03-101, F03-103, F03-105	10.99	MCU-508, EPB-519		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-038
F03-025	U14	F29P329SM-Q1	Other MCU functions (BLDC control, other peripherals)	Not counted for SG-03	U14		150.00	71%	106.500	n/a			·	·	·	·	n/a			·	·	·	·				Excluded rather than counted as safe: counting them would raise the SPFM without any design merit.	λ GATED OQ-007; share JUDGMENT
F03-030	U3	TPS653860-Q1	Watchdog or error monitor fails to act, or NRST cannot reset the MCU	Stop path for MCU faults lost (latent)	U3		40.00	8%	3.200	Latent	LM-05	90%	·	·	0.320	2.880	Latent	LM-05	90%	·	·	0.320	2.880	F03-020, F03-130	30.90	PMC-404, PMC-405, EPB-101	Partner: the MCU faults whose reaction is a PMIC reset (lockstep errors) and the clock faults the watchdog sees.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F03-031	U3	TPS653860-Q1	SAFE_OUT1 fails to assert in the safe state	MCU-independent stop lost (latent)	U3		40.00	3%	1.200	n/a			·	·	·	·	**Latent**	**LM-05**	90%	·	·	0.120	1.080	F03-021	1.50	EPB-408	SAFE_OUT1 is unconnected on VerB.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F03-034	U3	TPS653860-Q1	LDO1 (3.3 V, MCU I/O and U7 logic) regulates high	U14 and U7 logic overdriven: erratic outputs possible	U3		40.00	3%	1.200	**Direct**	SM-08	90%	·	**0.120**	·	1.080	**Direct**	SM-08	90%	·	**0.120**	·	1.080			PMC-206	The LDO1 overvoltage monitor sits in the same die as the regulator (OQ-002).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F03-035	U3	TPS653860-Q1	Rail monitors (EXT_VMON1 on the 1.25 V core, LDO overvoltage) stuck at 'good'	Supply overvoltage no longer detected (latent)	U3		40.00	3%	1.200	Latent	LM-05	90%	·	·	0.120	1.080	Latent	LM-05	90%	·	·	0.120	1.080	F03-110, F03-111, F03-034	3.72	PMC-312, PMC-317		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F03-032	U3	TPS653860-Q1	Spurious reset or safe state	No SG-03 effect (EPB unavailable)	U3		40.00	10%	4.000	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F03-033	U3	TPS653860-Q1	Other PMIC functions (regulators low or lost, pedal supplies, other monitors)	Not counted for SG-03	U3		40.00	73%	29.200	n/a			·	·	·	·	n/a			·	·	·	·				Loss of a rail resets U14 or removes EPB power: safe for SG-03. Regulators running high are F03-034 and the U4 rows.	λ GATED OQ-007; share JUDGMENT
F03-110	U4	TPS62902-Q1	1.25 V core regulated high (half of TI's 'output out of specification' mode)	U14 core overdriven: erratic commands possible (common to both lockstep cores)	U4		12.00	11%	1.320	**Direct**	SM-08	90%	·	**0.132**	·	1.188	**Direct**	SM-08	90%	·	**0.132**	·	1.188			PMC-303, PMC-315	TI's mode does not split high from low; half each is sev10's judgment.	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F03-111	U4	TPS62902-Q1	High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	U14 core overdriven: erratic commands possible (common to both lockstep cores)	U4		12.00	10%	1.200	**Direct**	SM-08	90%	·	**0.120**	·	1.080	**Direct**	SM-08	90%	·	**0.120**	·	1.080			PMC-301, PMC-302, PMC-304	PMC-304: the monitor must act before the U14 absolute maximum; timing not public (OQ-002).	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F03-112	U4	TPS62902-Q1	Output low or lost, low-side stuck on, power-FET damage, power-good and enable faults	No SG-03 effect (U14 brown-out reset; pins float and U7 turns off)	U4		12.00	79%	9.480	n/a			·	·	·	·	n/a			·	·	·	·			PMC-306, PMC-307, PMC-308	Shares from TI SFFS465A (22 % out of spec, 20 % FET stuck on, 36 % FET damage, 13 % PG, 9 % EN), less the two rows above. Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ JUDGMENT OQ-010
F03-120	U2	LM68645-Q1	High-side FET short: 12 V rail pulled toward 48V/12V_P	PMIC input overdriven: its outputs may run out of control	U2		20.00	10%	2.000	**Direct**	SM-09	90%	·	**0.200**	·	1.800	**Direct**	SM-09	90%	·	**0.200**	·	1.800			PMC-102, BCK-101	The CMPSS window removes 48V/12V_P, which also unpowers the EPB, in about 2 ms (SDAA375). U2 EN has no effect on a high-side short (PMC-102).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-014
F03-121	U2	LM68645-Q1	Output low or lost, regulation faults within the PMIC input range	No SG-03 effect (PMIC regulates or resets)	U2		20.00	90%	18.000	n/a			·	·	·	·	n/a			·	·	·	·			PMC-104, PMC-117	Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ GATED OQ-007; share JUDGMENT
F03-125	U1	LM74930-Q1	Other U1 faults (DGATE drive, current and voltage protection, IMON, pin shorts)	No SG-03 effect (48V/12V_P lost, or a protection against external surges lost)	U1		14.00	95%	13.300	n/a			·	·	·	·	n/a			·	·	·	·			SUP-209, SUP-305, SUP-311, SUP-401	An external surge is not a random hardware fault of this ECU; it is treated in the dependent-failure note. TI SFFS950 split, less the row below. Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	
F03-126	U1	LM74930-Q1	HGATE stuck high: Q1 cannot switch off	Overvoltage cut-off of SM-09 lost (latent)	U1		14.00	5%	0.700	Latent	LM-13	60%	·	·	0.280	0.420	Latent	LM-13	60%	·	·	0.280	0.420	F03-120	2.00	SUP-209, SUP-211	TI SFFS950 'HGATE stuck high' mode.	DC PROVISIONAL OQ-014
F03-127	Q1	SQJA90EP	Drain-source short: the input switch cannot open	Overvoltage cut-off of SM-09 lost (latent)	FET-80V		10.00	40%	4.000	Latent	LM-13	60%	·	·	1.600	2.400	Latent	LM-13	60%	·	·	1.600	2.400	F03-120	2.00	SUP-230		λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-014
F03-128	Q1	SQJA90EP	Open, gate-source short, on-resistance increase	No SG-03 effect (48V/12V_P lost or lossy)	FET-80V		10.00	60%	6.000	n/a			·	·	·	·	n/a			·	·	·	·			SUP-212	Counted n/a rather than Safe, as F03-125.	λ JUDGMENT OQ-010; share JUDGMENT (class split)
F03-130	Y1	CDC6C-Q1	Wrong frequency or poor accuracy	U14 timebase wrong: timing of the standstill check and of the command sequence wrong	Y1		3.00	30%	0.900	**Direct**	SM-21	90%	·	0.090	·	0.810	**Direct**	SM-21	90%	·	0.090	·	0.810			MCU-203, MCU-204	The U14 dual-clock comparator checks X1 against the internal oscillator continuously; errors inside its tolerance (about 3 %) cannot fake a standstill. TI SFFS685 split.	DC GATED OQ-007
F03-131	Y1	CDC6C-Q1	No output clock, or clock degraded (jitter, duty cycle)	No SG-03 effect (U14 missing-clock detection resets it; degraded clock stays within the PLL range)	Y1		3.00	70%	2.100	n/a			·	·	·	·	n/a			·	·	·	·			MCU-201, MCU-202	Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	
F03-132	R137	33 Ohm 0402	Open, short or drift of the clock series resistor	No SG-03 effect (open: clock lost, U14 reset)	RES-0402		0.30	100%	0.300	n/a			·	·	·	·	n/a			·	·	·	·			MCU-202	Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-040	U5	DRV3263-Q1	CUTOFF1 output stuck on	Q11 cannot be opened (latent)	U5		30.00	3%	0.900	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.090	0.810	F03-001, F03-003, F03-021	3.10	EPB-412	As built the cut-off serves no mechanism (R58 holds it on), so losing it changes nothing: Safe. With the actions it is the reaction of SM-03 and SM-04.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-029
F03-041	U5	DRV3263-Q1	CUTOFF1 output stuck off	No SG-03 effect (EPB unpowered)	U5		30.00	3%	0.900	Safe			·	·	·	·	Safe			·	·	·	·					λ GATED OQ-007; share JUDGMENT
F03-042	U5	DRV3263-Q1	Other gate-driver functions (BLDC bridge)	Not counted for SG-03	U5		30.00	94%	28.200	n/a			·	·	·	·	n/a			·	·	·	·				Counted under SG-01 and SG-02.	λ GATED OQ-007; share JUDGMENT
F03-045	C67	1 uF 25 V 0603	Short, leakage or open of the U5 charge-pump capacitor	No SG-03 effect (VCP low: Q11 under-driven or off, BLDC drive lost)	MLCC-0603G		0.50	100%	0.500	n/a			·	·	·	·	n/a			·	·	·	·			EPB-419	Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-050	Q11	SQJA90EP	Drain-source short	Cut-off cannot open (latent)	FET-80V		10.00	40%	4.000	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.400	3.600	F03-001, F03-003, F03-021	3.10	EPB-411	Safe as built: the cut-off serves no mechanism (R58).	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-029
F03-051	Q11	SQJA90EP	Drain-source open	No SG-03 effect (EPB unpowered)	FET-80V		10.00	20%	2.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-415		λ JUDGMENT OQ-010; share JUDGMENT (class split)
F03-052	Q11	SQJA90EP	Gate-source short	No SG-03 effect (Q11 off)	FET-80V		10.00	15%	1.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-414		λ JUDGMENT OQ-010; share JUDGMENT (class split)
F03-053	Q11	SQJA90EP	On-resistance increase	No SG-03 effect	FET-80V		10.00	25%	2.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-419		λ JUDGMENT OQ-010; share JUDGMENT (class split)
F03-055	Q6	BCR22PN	Collector-emitter short: the DRV3233-option drive holds the Q11 gate on	Cut-off cannot open (latent)	DTR		2.00	40%	0.800	Safe			·	·	·	·	n/a			·	·	·	·			EPB-404, EPB-405	Safe as built: the cut-off serves no mechanism. Q6 is not fitted with the actions (EPB-404, EPB-405).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-056	Q6	BCR22PN	Open or gain drift	No SG-03 effect	DTR		2.00	60%	1.200	Safe			·	·	·	·	n/a			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F03-057	R87	100 kOhm 0402	Open: no gate-source discharge	Q11 may stay on when CUTOFF1 releases (latent)	RES-0402		0.30	60%	0.180	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.018	0.162	F03-001, F03-003, F03-021	3.10	EPB-413	Safe as built: the cut-off serves no mechanism (R58).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-029
F03-058	R87	100 kOhm 0402	Short or drift	No SG-03 effect (short holds Q11 off)	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-059	R85	10 Ohm 0402	Open, short or drift of the Q11 gate resistor	No SG-03 effect (open: R87 turns Q11 off)	RES-0402		0.30	100%	0.300	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-060	R57	0 Ohm 0402	Open	No SG-03 effect (Q11 off, EPB unpowered)	RES-0R		0.10	100%	0.100	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-061	R58	0 Ohm 0402	Open	No SG-03 effect (restores the cut-off drive)	RES-0R		0.10	100%	0.100	Safe			·	·	·	·	n/a			·	·	·	·			EPB-401	R58 fitted is a design deficiency, not a random fault: it removes the reaction of SM-04 and the test LM-03 in scenario A. Not fitted in scenario B.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-062	R53, C63	0 Ohm 0402; 1 uF 25 V 0603	Open, short or drift on the DRV3233-option CUTOFF_ASCIN path	No SG-03 effect (acts only through Q6 and the cut-off)	MLCC-0603G		0.50	100%	0.500	Safe			·	·	·	·	n/a			·	·	·	·			EPB-406	Counted at the capacitor's class value for both parts. Not fitted with the actions (EPB-406).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-070	C96	4.7 uF 100 V 1210	Short, open or capacitance loss	No SG-03 effect (short: supply collapse, SG-07 rated in PCB-202)	MLCC-1210		2.00	100%	2.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-201, PCB-202		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-071	C97	0.1 uF 100 V 0603	Short, open or capacitance loss	No SG-03 effect	MLCC-0603		0.80	100%	0.800	Safe			·	·	·	·	Safe			·	·	·	·			EPB-201		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-072	C98	0.1 uF 0402	Short, open or capacitance loss on the U7 3.3 V pin	No SG-03 effect (U7 logic unsupplied: outputs off)	MLCC-0402		0.50	100%	0.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-117		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-073	C99	0.1 uF 0402	Short, open or capacitance loss on nFAULT	No SG-03 effect (short: permanent fault indication)	MLCC-0402		0.50	100%	0.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-119		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-074	C100	0.1 uF 0402	Short: Isense_EPB at 0 V	Unintended-motion monitor blind (latent)	MLCC-0402		0.50	50%	0.250	Latent	LM-02	90%	·	·	0.025	0.225	Latent	LM-02	90%	·	·	0.025	0.225	F03-003, F03-021	2.30	EPB-302		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-075	C100	0.1 uF 0402	Open or capacitance loss	No SG-03 effect (noisier reading)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-076	D12	BAT46W	Short, open or leakage of the Isense clamp	No SG-03 effect (short or leakage reads as current: false stop)	DIODE-SS		1.00	100%	1.000	Safe			·	·	·	·	Safe			·	·	·	·			EPB-307		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-077	R90	10 Ohm 0402	Open, short or drift of the DRVOFF series resistor	No SG-03 effect (open: U7 pull-up turns the bridge off)	RES-0402		0.30	100%	0.300	Safe			·	·	·	·	Safe			·	·	·	·			EPB-107		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-078	R91	10 kOhm 0402	Open, short or drift of the nSLEEP pull-up	No SG-03 effect (open: U7 sleeps)	RES-0402		0.30	100%	0.300	Safe			·	·	·	·	n/a			·	·	·	·			EPB-408	Replaced by the nSLEEP series resistor in scenario B (F03-092).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-079	R92	10 kOhm 0402	Open or short of the nFAULT pull-up	Fault reporting lost (latent)	RES-0402		0.30	70%	0.210	Latent	LM-06	90%	·	·	0.021	0.189	Latent	LM-06	90%	·	·	0.021	0.189	F03-006, F03-022	2.30	EPB-119		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-080	R92	10 kOhm 0402	Drift	No SG-03 effect	RES-0402		0.30	30%	0.090	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-081	R93	33 Ohm 0402	Open, short or drift on EN/IN1	No SG-03 effect (open: internal pull-down, no drive)	RES-0402		0.30	100%	0.300	Safe			·	·	·	·	Safe			·	·	·	·			EPB-112		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-082	R94	33 Ohm 0402	Open: PH/IN2 held by its internal pull-down	A commanded release drives the apply direction	RES-0402		0.30	60%	0.180	**Direct**	SM-06	60%	·	0.072	·	0.108	**Direct**	SM-06	90%	·	0.018	·	0.162			EPB-113	Rated for the apply direction (worst case; depends on the motor wiring).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-083	R94	33 Ohm 0402	Short or drift	No SG-03 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-084	R95	1 kOhm 0402	Short: Isense_EPB at 0 V	Unintended-motion monitor blind (latent)	RES-0402		0.30	10%	0.030	Latent	LM-02	90%	·	·	0.003	0.027	Latent	LM-02	90%	·	·	0.003	0.027	F03-003, F03-021	2.30	EPB-302		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-085	R95	1 kOhm 0402	Open or drift	No SG-03 effect (open reads as current: false stop)	RES-0402		0.30	90%	0.270	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-086	R96	33 Ohm 0402	Open: no U7 readback	Diagnostics of U7 blind (latent)	RES-0402		0.30	60%	0.180	Latent	LM-06	90%	·	·	0.018	0.162	Latent	LM-06	90%	·	·	0.018	0.162	F03-006, F03-022	2.30	EPB-514		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-087	R96	33 Ohm 0402	Short or drift	No SG-03 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-088	J5, J6	EPB motor wire pads	Open (crack, lift)	No SG-03 effect (EPB unavailable)	PAD	2	1.00	70%	0.700	Safe			·	·	·	·	Safe			·	·	·	·			EPB-207		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-089	J5, J6	EPB motor wire pads	Short to an adjacent pad or to the harness	A second terminal short can drive the motor without U7 (latent)	PAD	2	1.00	30%	0.300	Latent	LM-07	60%	·	·	0.120	0.180	Latent	LM-07	60%	·	·	0.120	0.180	F03-089, F03-012	1.30	EPB-205, EPB-206, EPB-314		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-140	R133, R135	33 Ohm 0402 (SDI, CLK)	Open or drift: SPI-D transfers to U7 and U6 fail	U7 configuration and readback over SPI lost (latent)	RES-0402	2	0.60	90%	0.540	Latent	LM-06	90%	·	·	0.054	0.486	Latent	LM-06	90%	·	·	0.054	0.486	F03-006, F03-022	2.30	EPB-502, EPB-511, EPB-519	Pin control of U7 (DRVOFF, EN/IN1, PH/IN2) is unaffected.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-141	R133, R135	33 Ohm 0402 (SDI, CLK)	Short	No SG-03 effect (series termination bypassed)	RES-0402	2	0.60	10%	0.060	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-142	R89	33 Ohm 0402 (U6 SDO)	Open, short or drift	No SG-03 effect (U6 readback lost; standstill is taken from the WSSO pulses, never from SPI data)	RES-0402		0.30	100%	0.300	n/a			·	·	·	·	n/a			·	·	·	·			EPB-519	Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-090	New (EPB-121)	10 kOhm DRVOFF pull-up	Open: DRVOFF floats while the MCU pins float	Stop path for MCU faults weakened (latent)	RES-0402		0.30	60%	0.180	n/a			·	·	·	·	**Latent**	**LM-01**	90%	·	·	0.018	0.162	F03-020, F03-021	31.50	EPB-121		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-091	New (EPB-121)	10 kOhm DRVOFF pull-up	Short or drift	No SG-03 effect (short holds DRVOFF high: EPB unavailable)	RES-0402		0.30	40%	0.120	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-092	New (EPB-408)	1 kOhm nSLEEP series resistor	Short: SAFE_OUT1 cannot override the MCU drive on nSLEEP	MCU-independent stop lost (latent)	RES-0402		0.30	10%	0.030	n/a			·	·	·	·	**Latent**	**LM-05**	90%	·	·	0.003	0.027	F03-021	1.50	EPB-408		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F03-093	New (EPB-408)	1 kOhm nSLEEP series resistor	Open or drift	No SG-03 effect (open: U7 sleeps)	RES-0402		0.30	90%	0.270	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-094	New (EPB-211)	OUTA/OUTB divider resistors	Open or drift: terminal readback wrong	Independent terminal monitor blind (latent)	RES-0402	4	1.20	90%	1.080	n/a			·	·	·	·	**Latent**	**LM-02**	90%	·	·	0.108	0.972	F03-001	0.80	EPB-211, EPB-314	Checked at each commanded operation like the current sense.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F03-095	New (EPB-211)	OUTA/OUTB divider resistors	Short: readback at a rail	No SG-03 effect (reads as motion: false stop)	RES-0402	4	1.20	10%	0.120	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F03-100	U6	WSS001-Q1	Standstill reported while the wheel turns (decoder fault, false standstill flag)	Static EPB apply permitted while moving	U6		15.00	20%	3.000	**Direct**	SM-07	99%	·	0.030	·	2.970	**Direct**	SM-07	99%	·	0.030	·	2.970			WSS-315, WSS-118		λ UNRELEASED OQ-008; share UNRELEASED; DC PROVISIONAL OQ-038
F03-101	U6	WSS001-Q1	No speed pulses although the wheel turns (unsupplied, output static)	Static EPB apply permitted while moving	U6		15.00	30%	4.500	**Direct**	SM-07	99%	·	0.045	·	4.455	**Direct**	SM-07	99%	·	0.045	·	4.455			WSS-103, WSS-107		λ UNRELEASED OQ-008; share UNRELEASED; DC PROVISIONAL OQ-038
F03-102	U6	WSS001-Q1	Other faults (speed too high, SPI loss) without a false standstill	Not counted for SG-03	U6		15.00	50%	7.500	n/a			·	·	·	·	n/a			·	·	·	·				Counted under SG-05.	λ UNRELEASED OQ-008; share UNRELEASED
F03-105	C92	0.1 uF 0402 (U6 5 V)	Short: 5 V rail pulled down (U6 and both CAN transceivers unsupplied)	Static EPB apply permitted while moving (no pulses)	MLCC-0402		0.50	50%	0.250	**Direct**	SM-07	99%	·	0.003	·	0.248	**Direct**	SM-07	99%	·	0.003	·	0.248			PMC-207	The rule 'loss of pulses is invalid, never standstill' does not need the CAN bus that this fault also takes down.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-038
F03-106	C92	0.1 uF 0402 (U6 5 V)	Open or capacitance loss	No SG-03 effect	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-107	C89, C91	0.1 uF 0402 (U6 12 V, 3.3 V)	Short, open or capacitance loss	No SG-03 effect (short collapses the 12 V or 3.3 V rail: corner off)	MLCC-0402	2	1.00	100%	1.000	n/a			·	·	·	·	n/a			·	·	·	·				Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F03-103	WSS front end	D5, R84, R86, R88, C88, C90, C93-C95, J1, J2	Open, short or clamp failure that stops the sensor pulses	Static EPB apply permitted while moving	WSS-FE		5.40	60%	3.240	**Direct**	SM-07	99%	·	0.032	·	3.208	**Direct**	SM-07	99%	·	0.032	·	3.208			WSS-202 to WSS-209, WSS-301	Aggregated for SG-03; the part-level split is on the SG-05 tab.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-038
F03-104	WSS front end	D5, R84, R86, R88, C88, C90, C93-C95, J1, J2	Faults without loss of pulses	No SG-03 effect	WSS-FE		5.40	40%	2.160	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F03-150	U8, U10	TCAN1043H-Q1	Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	No SG-03 effect (frames lost or rejected by their CRC; speed invalid, EPB static apply not permitted)	TCAN	2	18.00	98%	17.640	n/a			·	·	·	·	n/a			·	·	·	·			CAN-104, CAN-105, CAN-201, CAN-203	A transceiver cannot create a CRC-valid frame that reports standstill. TI SLLA525A split, less the row below. Counted n/a rather than Safe: these faults have no path to the goal, and counting them would raise the SPFM without design merit.	share JUDGMENT
F03-151	U8, U10	TCAN1043H-Q1	Transceiver stays awake when nSTB_CAN goes low (INH held high)	Overvoltage cut-off of SM-09 lost (latent)	TCAN	2	18.00	2%	0.360	Latent	LM-13	60%	·	·	0.144	0.216	Latent	LM-13	60%	·	·	0.144	0.216	F03-120	2.00	CAN-119, CAN-412, CAN-416	Part of TI's 5 % pin-short mode (sev10 judgment). The key-off cut-off test (LM-13) finds it.	share JUDGMENT; DC PROVISIONAL OQ-014
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**121.08 λ**			**2.300**	**1.694**	**5.635**	**71.831**	**121.18 λ**			**0.000**	**1.630**	**6.392**	**81.008**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-04 · Computed (Rev A, provisional)

ASIL C

Avoid loss of parking or standstill hold while the vehicle is stationary

Safe state: Hold maintained or re-applied; driver warned; transmission park lock if fitted

FTTI: TBD; provisional 1 s (ASSUMED) · Hazardous events: HE-14, HE-15 (S10-QLN-HARA-001 Rev B)

	SPFM · target ≥ 97%	LFM · target ≥ 80%	PMHF (FIT) · item < 100 FIT; corner share open (OQ-046)
As built	94.02%	94.86%	6.17
With actions	95.60%	94.40%	4.63

Key findings

1. As built, SG-04 has one single-point fault: a U7 output stage that drives the release direction on its own. Nothing observes the motor terminals independently of U7, the IPROPI mirror is blind to a shorted high-side FET, and the only stop outside the die (Q11) cannot open because R58 ties its gate to the bus. U7 is the only drive path, so the corner cannot re-clamp: the hold must come from the other rear corner (EPB-211, EPB-314, EPB-401). U14 EPB pins stuck in the release state are covered only by a report to the other corner (SM-40, Low as built).

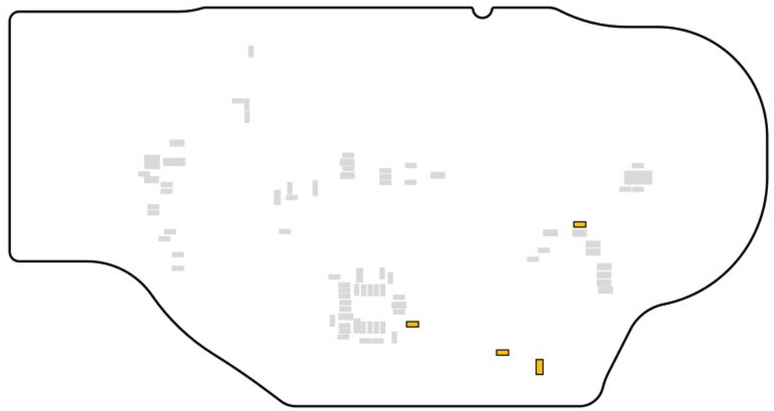
2. With the actions SG-04 still misses its SPFM target (95.6 % against 97 %; 94.0 % as built) on the ASSUMED data. The dominant residual is not unintended release but the faults that leave the EPB unable to apply (U7 outputs off, Q11 open, pads open), whose apply-completion check is capped at Medium, and the faults that end an apply early on a false stall: a current reading that is too high (D12 short or leakage, R95 open, IPROPI gain). SG-03 treats a high reading as safe-side; for SG-04 it is the hazard, and only gross errors are seen without a second current or force measurement (EPB-309, EPB-318). Closing the gap needs that second measurement, or High coverage of the no-drive faults. The vehicle answer on single-corner hold (OQ-052) decides whether a detected no-apply at one corner reaches the safe state at all.

3. The safe states of SG-03 (release, inhibit apply) and SG-04 (hold) conflict, and so do SG-01's (release to zero force on a request timeout, CAN-102; release first after a PMIC reset, PMC-419) if the standstill hold uses the service brake. Every fault reaction needs an arbitration that holds unless independent motion is confirmed; a false "moving" at standstill must not turn an SG-03 reaction into a release. The Q11 cut-off helps SG-04 (it stops a release and the spindle keeps the rest) but removes the only way to re-clamp this corner.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Elements that can release the EPB at standstill, or leave it without holding force after a park or auto-hold apply (HE-14, HE-15): the EPB driver U7 and its passives, the Q11 cut-off and its drive (U5 CUTOFF1, R57, R85, R87, C67), the motor pads J5/J6, the current-sense path (R95, C100, D12, the U14 ADC channel), the shared SPI-D resistors, the parts of the MCU (U14) that command the EPB or receive a release request, the PMIC (U3) supervision, the rails whose overvoltage can corrupt U14 (U4, U3 LDO1, U2) with the U1/Q1/INH cut-off path, and the parts added by the DFMEA actions. These are the SG-03 parts classified for release instead of apply. The spindle is self-locking (A-06, OQ-023): a fault that removes EPB power while the EPB holds is harmless, and matters only at the next apply, where it is Direct and controlled by the apply-completion check (SM-41) before the driver leaves. When the vehicle is parked and the bus asleep the transceivers drop INH and U1 removes 48V/12V_P, so no powered release is possible; the exposure is the time awake at standstill (auto-hold, the park transition, wake-ups). Faults that take the whole corner down (rail loss, 3.3 V or VM short through the U1 breaker) are counted under SG-02 as on SG-01 and are n/a here; the brake controller's status timeout is the vehicle reaction. Wheel-speed and standstill information (U6, its front end) and the clock (Y1) are left out: this FMEDA assumes a fault or a lost standstill confirmation never releases a hold (OQ-053). Q6, R53, C63 and R58 have no SG-04 path (they only decide whether the cut-off can open) and are left out. Motor wires swapped at J5/J6 (EPB-224) and firmware settings (EPB-213, EPB-313, EPB-321) are systematic faults, not rows here.

Failure modes											VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F04-001	U7	DRV8263-Q1	Faults that add force or remove a protection unrelated to release: output stage drives the apply direction without a command (F03-001, 0.04), thermal protection lost (F03-013, 0.05), OUTx short on the terminal driven only for release (half of F03-012, 0.025)	No SG-04 effect (force added or release blocked: SG-03, SG-07, HE-17 QM)	U7		20.00	12%	2.300	Safe			·	·	·	·	Safe			·	·	·	·			EPB-211, EPB-214, EPB-203	An apply-direction drive at standstill adds force to stall; it cannot remove the hold. A short that blocks only the release direction leaves the apply intact.	λ GATED OQ-007; share JUDGMENT
F04-002	U7	DRV8263-Q1	Output stage drives the release direction without a command (diagonal FET pair shorted or gate drive stuck on)	EPB released while the vehicle is held: rolls away (HE-14, HE-15)	U7		20.00	4%	0.800	**Direct**			**0.800**	·	·	·	**Direct**	**SM-04**	90%	·	0.080	·	0.720			EPB-211, EPB-314	Share as F03-002. As built no mechanism acts: DRVOFF is in the failed die, the IPROPI mirror is blind to a shorted high-side FET and Q11 cannot open (R58). With the actions the terminal readback opens Q11 (STOP) and reports (HAND). U7 is the only drive path: no re-clamp at this corner. Credit assumes the stop plus the other corner's re-clamp hold the vehicle within 1 s (OQ-052).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-029
F04-003	U7	DRV8263-Q1	Input logic fault (EN/IN1 or PH/IN2 buffer, state machine) drives the bridge in the release direction without a command	EPB released while the vehicle is held	U7		20.00	3%	0.600	**Direct**	SM-03	60%	·	**0.240**	·	0.360	**Direct**	SM-03	90%	·	0.060	·	0.540			EPB-103	F03-003 (0.04) split: 0.03 here, 0.01 in F04-014. Current flows through gate-driven FETs, so IPROPI sees it. As built the stop (DRVOFF) acts in the same die: Low. With the actions Q11 opens (STOP). U7 logic is faulty: no re-clamp at this corner (HAND).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-014	U7	DRV8263-Q1	Input logic fault inverts the direction: a commanded apply drives the release end stop and ends on a stall	Apply reported complete with no holding force (HE-14)	U7		20.00	1%	0.200	**Direct**	SM-06	60%	·	0.080	·	0.120	**Direct**	SM-06	90%	·	0.020	·	0.180			EPB-104, EPB-113	Part of F03-003. As built the direction is inferred from the current profile (an end-stop stall has no force ramp); with the actions from the terminal voltages. Reaction: apply reported failed, HAND.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-004	U7	DRV8263-Q1	DRVOFF no longer disables the bridge	Stop path for an erroneous U14 release command weakened (latent)	U7		20.00	6%	1.200	Latent	LM-01	90%	·	·	0.120	1.080	Latent	LM-01	90%	·	·	0.120	1.080	F04-020	30.00	EPB-102, EPB-105	Kept latent as on SG-03 (F03-004). Conservative: when the U14 pins float after a lockstep reset, the EN/IN1 pull-down also puts the bridge in brake.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-005	U7	DRV8263-Q1	Current-sense output (IPROPI) reads low or zero	Unintended-release monitor blind (latent)	U7		20.00	5%	1.000	Latent	LM-02	90%	·	·	0.100	0.900	Latent	LM-02	90%	·	·	0.100	0.900	F04-003, F04-021	2.10	EPB-319	F03-005 (0.08) split: 0.05 low or zero here, 0.03 high in F04-015. A low reading also makes an apply look failed (safe side).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-015	U7	DRV8263-Q1	Current-sense output (IPROPI) reads high (gain or offset error)	Apply ends on a false stall below holding force (HE-14)	U7		20.00	3%	0.600	**Direct**	SM-42	60%	·	**0.240**	·	0.360	**Direct**	SM-42	60%	·	**0.240**	·	0.360			EPB-318	The rest-offset check sees an offset; a gain error is seen only when gross (no second current or force measurement).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-043
F04-006	U7	DRV8263-Q1	Register corruption unlocks SPI control and drives the release, or lowers OCP_SEL/S_ITRIP so the apply stops below holding force	EPB released, or held below holding force	U7		20.00	4%	0.800	**Direct**	SM-05	90%	·	0.080	·	0.720	**Direct**	SM-05	90%	·	0.080	·	0.720			EPB-501, EPB-502, EPB-504, EPB-516	Share as F03-006. Readback within 100 ms; reaction rewrites and locks the registers and re-applies (RECLAMP), else HAND.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-007	U7	DRV8263-Q1	Fault reporting (nFAULT, STATUS, SPI readback) lost or wrong	Diagnostics of U7 blind (latent)	U7		20.00	10%	2.000	Latent	LM-06	90%	·	·	0.200	1.800	Latent	LM-06	90%	·	·	0.200	1.800	F04-006, F04-022	2.30	EPB-507, EPB-509		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-008	U7	DRV8263-Q1	Outputs off or high impedance; the bridge cannot drive	EPB held: none (self-locking). EPB released: the next park or auto-hold apply fails (HE-14)	U7		20.00	30%	6.000	**Direct**	SM-41	90%	·	**0.600**	·	5.400	**Direct**	SM-41	90%	·	**0.600**	·	5.400			EPB-209, EPB-212	Share as F03-008 (Safe for SG-03). No current on the commanded apply; U7 is the only drive path, so the reaction is HAND before the driver leaves.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-009	U7	DRV8263-Q1	VM or GND pin short, internal supply short	Corner supply pulled into the U1 breaker: whole corner lost	U7		20.00	5%	1.000	n/a			·	·	·	·	n/a			·	·	·	·			EPB-201	A held EPB keeps its force. Corner loss is counted under SG-02 (as SG-01); the brake controller's timeout is the vehicle reaction. Counted n/a rather than Safe.	λ GATED OQ-007; share JUDGMENT
F04-012	U7	DRV8263-Q1	OUTA or OUTB shorted to VM or GND on the terminal the apply must drive	The next apply trips OCP or cannot drive: no hold (HE-14)	U7		20.00	3%	0.500	**Direct**	SM-41	90%	·	0.050	·	0.450	**Direct**	SM-41	90%	·	0.050	·	0.450			EPB-203	Half of F03-012 (0.05); the other half blocks only the release (F04-001). With over-current protection lost (F04-010), a VM short on this terminal in the brake state drives the release.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-010	U7	DRV8263-Q1	Over-current protection lost	A terminal short then drives the motor from the brake state, possibly in release (latent)	U7		20.00	5%	1.000	Latent			·	·	1.000	·	Latent			·	·	1.000	·	F04-012, F04-099	0.80	EPB-221	No test of the over-current protection exists, so the full λ counts as latent (as F03-010).	λ GATED OQ-007; share JUDGMENT
F04-011	U7	DRV8263-Q1	Other internal faults (charge pump, oscillator, SPI timing, POR on defaults) that stop the bridge	The next apply fails (HE-14)	U7		20.00	10%	2.000	**Direct**	SM-41	90%	·	**0.200**	·	1.800	**Direct**	SM-41	90%	·	**0.200**	·	1.800			EPB-212, EPB-216, EPB-503	Share as F03-011 (Safe for SG-03). HAND.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F04-020	U14	F29P329SM-Q1	CPU, memory or bus fault produces an erroneous EPB release command	EPB released while the vehicle is held	U14		150.00	20%	30.000	**Direct**	SM-01	99%	·	**0.300**	·	29.700	**Direct**	SM-01	99%	·	**0.300**	·	29.700			EPB-101, MCU-503	Same 20 % share as F03-020: the logic that computes the EPB command, counted on each goal for the direction that violates it. The lockstep reset floats the pins: U7 goes Hi-Z (DRVOFF pull-up) and the spindle keeps the force (STOP within microseconds). After restart U14 re-applies (RECLAMP) if the EPB state survives the reset (EPB-315).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F04-021	U14	F29P329SM-Q1	EPB control pins (U14.2 DRVOFF, U14.11, U14.98) stuck in the release-drive state (port fault the lockstep does not see)	EPB released while the vehicle is held	U14		150.00	1%	1.500	**Direct**	SM-40	60%	·	**0.600**	·	0.900	**Direct**	SM-40	90%	·	**0.150**	·	1.350			EPB-101, EPB-408	Share as F03-021. Unlike SG-03, the reaction does not need the stuck pins: U14 sees current with no command and reports (HAND). As built the release runs to its end stop; with the actions Q11 and SAFE_OUT1 also stop it (STOP). No re-clamp at this corner through stuck pins.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-027	U14	F29P329SM-Q1	PH/IN2 drive pin (U14.98) stuck at the release level	A commanded apply drives the release end stop and is reported complete (HE-14)	U14		150.00	1%	0.750	**Direct**	SM-06	60%	·	**0.300**	·	0.450	**Direct**	SM-06	90%	·	0.075	·	0.675			EPB-113, MCU-407	Taken from the U14 'other' share. HAND.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-028	U14	F29P329SM-Q1	EPB control pins stuck in the off state (DRVOFF high or EN/IN1 low)	The next apply fails (HE-14)	U14		150.00	1%	0.750	**Direct**	SM-41	90%	·	0.075	·	0.675	**Direct**	SM-41	90%	·	0.075	·	0.675			EPB-106, EPB-111	Taken from the U14 'other' share. HAND.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-022	U14	F29P329SM-Q1	SPI-D peripheral fault writes wrong data to U7	EPB released, or held below holding force	U14		150.00	1%	1.500	**Direct**	SM-05	90%	·	**0.150**	·	1.350	**Direct**	SM-05	90%	·	**0.150**	·	1.350			EPB-512, EPB-517	Share as F03-022.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-023	U14	F29P329SM-Q1	Lockstep comparator, ECC or error-signal module fault	MCU self-monitoring blind (latent)	U14		150.00	5%	7.500	Latent	LM-04	90%	·	·	0.750	6.750	Latent	LM-04	90%	·	·	0.750	6.750	F04-020	30.00	MCU-504, MCU-505, MCU-506		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F04-024	U14	F29P329SM-Q1	Isense_EPB ADC channel reads low or zero	Unintended-release monitor blind (latent)	U14		150.00	1%	0.750	Latent	LM-02	90%	·	·	0.075	0.675	Latent	LM-02	90%	·	·	0.075	0.675	F04-003, F04-021	2.10	EPB-302	F03-024 (0.01) split: 0.005 low here, 0.005 high in F04-029.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-029	U14	F29P329SM-Q1	Isense_EPB ADC channel reads high	Apply ends on a false stall below holding force (HE-14)	U14		150.00	1%	0.750	**Direct**	SM-42	60%	·	**0.300**	·	0.450	**Direct**	SM-42	60%	·	**0.300**	·	0.450			EPB-316, EPB-320		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-043
F04-026	U14	F29P329SM-Q1	CAN receive path (MCAN, message RAM) delivers a false EPB release or drive-away request	EPB released while the vehicle is held	U14		150.00	1%	1.500	**Direct**	SM-43	90%	·	**0.150**	·	1.350	**Direct**	SM-43	90%	·	**0.150**	·	1.350			MCU-508, CAN-101	Same share as F03-026 (the CAN receive path). Message-RAM ECC catches bit errors; the E2E check on the payload catches the rest, and the hold is kept.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-040
F04-025	U14	F29P329SM-Q1	Other MCU functions (BLDC control, other peripherals)	Not counted for SG-04	U14		150.00	69%	103.500	n/a			·	·	·	·	n/a			·	·	·	·				Excluded rather than counted as safe. F04-155 (CAN transmit) is the remaining U14 share.	λ GATED OQ-007; share JUDGMENT
F04-030	U3	TPS653860-Q1	Watchdog or error monitor fails to act, or NRST cannot reset the MCU	Stop path for MCU faults lost (latent)	U3		40.00	8%	3.200	Latent	LM-05	90%	·	·	0.320	2.880	Latent	LM-05	90%	·	·	0.320	2.880	F04-020	30.00	PMC-404, PMC-405, EPL101	Share as F03-030. Clock faults are not a row here (scope), so the partner is the lockstep row only.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F04-034	U3	TPS653860-Q1	LDO1 (3.3 V, MCU I/O and U7 logic) regulates high	U14 and U7 logic overdriven: an erratic release possible	U3		40.00	3%	1.200	**Direct**	SM-08	90%	·	**0.120**	·	1.080	**Direct**	SM-08	90%	·	**0.120**	·	1.080			PMC-206	The reset floats the pins and U7 goes Hi-Z: STOP keeps the force. The LDO1 monitor sits in the same die as the regulator (OQ-002).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F04-035	U3	TPS653860-Q1	Rail monitors (EXT_VMON1 on the 1.25 V core, LDO overvoltage) stuck at 'good'	Supply overvoltage no longer detected (latent)	U3		40.00	3%	1.200	Latent	LM-05	90%	·	·	0.120	1.080	Latent	LM-05	90%	·	·	0.120	1.080	F04-110, F04-111, F04-034	3.72	PMC-312, PMC-317		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F04-032	U3	TPS653860-Q1	Spurious reset or safe state	EPB held: none (U7 Hi-Z). During an apply: the apply stops short (HE-14)	U3		40.00	10%	4.000	**Direct**	SM-41	90%	·	**0.400**	·	3.600	**Direct**	SM-41	90%	·	**0.400**	·	3.600			EPB-315	Safe for SG-03 (F03-032). Conservative: only a reset inside the apply window matters, and the pending park request usually re-applies. A latched safe state silences the corner (SG-02).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-033	U3	TPS653860-Q1	Other PMIC functions (regulators low or lost, pedal supplies, other monitors, SAFE_OUT1 failing to assert)	Not counted for SG-04	U3		40.00	76%	30.400	n/a			·	·	·	·	n/a			·	·	·	·				F03-033 (0.73) plus F03-031 (0.03). SAFE_OUT1 serves no SG-04 mechanism (the credited reactions do not rely on it). A lost rail takes the corner down (SG-02); a held EPB keeps its force.	λ GATED OQ-007; share JUDGMENT
F04-040	U5	DRV3263-Q1	CUTOFF1 output stuck on	Q11 cannot be opened: the stop of an unintended release is lost	U5		30.00	3%	0.900	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.090	0.810	F04-002, F04-003	1.40	EPB-412	As built the cut-off serves no mechanism (R58). With the actions it is the STOP of SM-03 and SM-04. F04-021 relies on the report (SM-40), not on Q11, and is not a partner.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-029
F04-041	U5	DRV3263-Q1	CUTOFF1 output stuck off	With the actions: Q11 off, EPB unpowered; the next apply fails (HE-14)	U5		30.00	3%	0.900	Safe			·	·	·	·	**Direct**	**SM-41**	90%	·	0.090	·	0.810			EPB-416	As built R58 holds Q11 on whatever CUTOFF1 does (EPB-403). Safe for SG-03.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-032
F04-042	U5	DRV3263-Q1	Other gate-driver functions (BLDC bridge)	Not counted for SG-04	U5		30.00	94%	28.200	n/a			·	·	·	·	n/a			·	·	·	·				Counted under SG-01 and SG-02.	λ GATED OQ-007; share JUDGMENT
F04-045	C67	1 uF 25 V 0603	Short, leakage or open of the U5 charge-pump capacitor	With the actions: Q11 under-driven or off; the next apply fails or runs weak (HE-14)	MLCC-0603G		0.50	100%	0.500	n/a			·	·	·	·	**Direct**	**SM-41**	90%	·	0.050	·	0.450			EPB-419	As built Q11 is driven through R58, not from VCP: no SG-04 path (BLDC drive lost, SG-02).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-050	Q11	SQJA90EP	Drain-source short	Cut-off cannot open: the stop of an unintended release is lost (latent)	FET-80V		10.00	40%	4.000	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.400	3.600	F04-002, F04-003	1.40	EPB-411	Safe as built: the cut-off serves no mechanism (R58).	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-029
F04-051	Q11	SQJA90EP	Drain-source open	EPB unpowered: held force kept, the next apply fails (HE-14)	FET-80V		10.00	20%	2.000	**Direct**	SM-41	90%	·	**0.200**	·	1.800	**Direct**	SM-41	90%	·	**0.200**	·	1.800			EPB-415	Safe for SG-03. U7 VMUV and no current on the apply; HAND.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-052	Q11	SQJA90EP	Gate-source short	Q11 off: held force kept, the next apply fails (HE-14)	FET-80V		10.00	15%	1.500	**Direct**	SM-41	90%	·	**0.150**	·	1.350	**Direct**	SM-41	90%	·	**0.150**	·	1.350			EPB-414	As EPB-414: not detected at idle, only at the apply; HAND.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-053	Q11	SQJA90EP	On-resistance increase	No SG-04 effect	FET-80V		10.00	25%	2.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-419	A few mOhm against the motor winding does not move the stall current; a gross increase shows as an apply that times out (SM-41).	λ JUDGMENT OQ-010; share JUDGMENT (class split)
F04-057	R87	100 kOhm 0402	Open: no gate-source discharge	Q11 may stay on when CUTOFF1 releases (latent)	RES-0402		0.30	60%	0.180	Safe			·	·	·	·	**Latent**	**LM-03**	90%	·	·	0.018	0.162	F04-002, F04-003	1.40	EPB-413	Safe as built: the cut-off serves no mechanism (R58).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-029
F04-058	R87	100 kOhm 0402	Short or drift	Short holds Q11 off: the next apply fails (HE-14)	RES-0402		0.30	40%	0.120	**Direct**	SM-41	90%	·	0.012	·	0.108	**Direct**	SM-41	90%	·	0.012	·	0.108			EPB-414	Drift has no effect; counted with the short (conservative).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-060	R57	0 Ohm 0402	Open	Q11 off (R87 discharges the gate): the next apply fails (HE-14)	RES-0R		0.10	100%	0.100	**Direct**	SM-41	90%	·	0.010	·	0.090	**Direct**	SM-41	90%	·	0.010	·	0.090			EPB-416	Safe for SG-03 (F03-060).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-070	C98	0.1 uF 0402	Short on the U7 3.3 V pin	3.3 V rail collapses: corner reset	MLCC-0402		0.50	50%	0.250	n/a			·	·	·	·	n/a			·	·	·	·			EPB-117	Corner loss, counted under SG-02. Counted n/a rather than Safe.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-071	C98	0.1 uF 0402	Open or capacitance loss on the U7 3.3 V pin	U7 logic supply glitches: an apply stops short (HE-14)	MLCC-0402		0.50	50%	0.250	**Direct**	SM-41	90%	·	0.025	·	0.225	**Direct**	SM-41	90%	·	0.025	·	0.225			EPB-118	FAULT.POR and no stall within the window; the pending apply is repeated or reported.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-072	C99	0.1 uF 0402	Short, open or capacitance loss on nFAULT	No SG-04 effect (short: permanent fault indication, EPB reported unavailable)	MLCC-0402		0.50	100%	0.500	Safe			·	·	·	·	Safe			·	·	·	·			EPB-119		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-073	C100	0.1 uF 0402	Short: Isense_EPB at 0 V	Unintended-release monitor blind (latent)	MLCC-0402		0.50	50%	0.250	Latent	LM-02	90%	·	·	0.025	0.225	Latent	LM-02	90%	·	·	0.025	0.225	F04-003, F04-021	2.10	EPB-302	An apply then shows no inrush and is reported failed (safe side).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-074	C100	0.1 uF 0402	Open or capacitance loss	No SG-04 effect (noisier reading)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·			EPB-308		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-075	D12	BAT46W	Short or leakage of the Isense clamp	Isense reads high: the apply ends on a false stall below holding force (HE-14)	DIODE-SS		1.00	70%	0.700	**Direct**	SM-42	60%	·	**0.280**	·	0.420	**Direct**	SM-42	60%	·	**0.280**	·	0.420			EPB-304, EPB-306	Safe for SG-03 (a false stop); the hazard for SG-04. A short (full scale) fails the rest-offset check reliably; hot leakage is partly compensated by the offset subtraction, not during self-heating.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-043
F04-076	D12	BAT46W	Open	No SG-04 effect (ADC input clamp lost)	DIODE-SS		1.00	30%	0.300	Safe			·	·	·	·	Safe			·	·	·	·			EPB-307		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-077	R85, R90, R93	10 Ohm, 10 Ohm, 33 Ohm 0402 (Q11 gate, DRVOFF, EN/IN1)	Open: Q11 off (R85), DRVOFF held high by the U7 pull-up (R90), EN/IN1 held low (R93)	Bridge cannot drive: the next apply fails (HE-14)	RES-0402	3	0.90	60%	0.540	**Direct**	SM-41	90%	·	0.054	·	0.486	**Direct**	SM-41	90%	·	0.054	·	0.486			EPB-106, EPB-111, EPB-416	Safe for SG-03.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F04-078	R85, R90, R93	10 Ohm, 10 Ohm, 33 Ohm 0402 (Q11 gate, DRVOFF, EN/IN1)	Short or drift	No SG-04 effect	RES-0402	3	0.90	40%	0.360	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-079	R91	10 kOhm 0402	Open: nSLEEP pulled low by the U7 pull-down	U7 asleep: the next apply fails (HE-14)	RES-0402		0.30	60%	0.180	**Direct**	SM-41	90%	·	0.018	·	0.162	n/a			·	·	·	·			EPB-108	Replaced by the nSLEEP series resistor in scenario B (F04-092).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-080	R91	10 kOhm 0402	Short or drift	No SG-04 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	n/a			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-081	R92	10 kOhm 0402	Open or short of the nFAULT pull-up	Fault reporting lost (latent)	RES-0402		0.30	70%	0.210	Latent	LM-06	90%	·	·	0.021	0.189	Latent	LM-06	90%	·	·	0.021	0.189	F04-006, F04-022	2.30	EPB-119		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-082	R92	10 kOhm 0402	Drift	No SG-04 effect	RES-0402		0.30	30%	0.090	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-083	R94	33 Ohm 0402	Open: PH/IN2 held by its internal pull-down	A commanded apply drives the release end stop and is reported complete (HE-14)	RES-0402		0.30	60%	0.180	**Direct**	SM-06	60%	·	0.072	·	0.108	**Direct**	SM-06	90%	·	0.018	·	0.162			EPB-113	Rated for the release direction (worst case for SG-04; SG-03 rates the same share for apply, F03-082). Depends on the motor wiring.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-084	R94	33 Ohm 0402	Short or drift	No SG-04 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-085	R95	1 kOhm 0402	Open: Isense_EPB drifts toward full scale	Apply ends on a false stall below holding force (HE-14)	RES-0402		0.30	60%	0.180	**Direct**	SM-42	60%	·	0.072	·	0.108	**Direct**	SM-42	60%	·	0.072	·	0.108			EPB-303	Safe for SG-03 (F03-085). Minimum run time before a stall is accepted catches it at the first apply.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-043
F04-086	R95	1 kOhm 0402	Short: Isense_EPB at 0 V	Unintended-release monitor blind (latent)	RES-0402		0.30	10%	0.030	Latent	LM-02	90%	·	·	0.003	0.027	Latent	LM-02	90%	·	·	0.003	0.027	F04-003, F04-021	2.10	EPB-302		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-087	R95	1 kOhm 0402	Drift (reading scaled high or low)	Reading high: apply ends below holding force (HE-14)	RES-0402		0.30	30%	0.090	**Direct**	SM-42	60%	·	0.036	·	0.054	**Direct**	SM-42	60%	·	0.036	·	0.054			EPB-309	Only upward drift matters (downward adds force); the whole drift share is counted, conservatively.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-043
F04-088	R96	33 Ohm 0402	Open: no U7 readback	Diagnostics of U7 blind (latent)	RES-0402		0.30	60%	0.180	Latent	LM-06	90%	·	·	0.018	0.162	Latent	LM-06	90%	·	·	0.018	0.162	F04-006, F04-022	2.30	EPB-514		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-089	R96	33 Ohm 0402	Short or drift	No SG-04 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-098	J5, J6	EPB motor wire pads	Open (crack, lift)	Held force kept; the next apply fails (HE-14)	PAD	2	1.00	70%	0.700	**Direct**	SM-41	90%	·	0.070	·	0.630	**Direct**	SM-41	90%	·	0.070	·	0.630			EPB-207	Safe for SG-03. No current on the commanded apply; HAND.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-099	J5, J6	EPB motor wire pads	Short to an adjacent pad or to the harness	The next apply trips OCP or cannot drive (HE-14)	PAD	2	1.00	30%	0.300	**Direct**	SM-41	90%	·	0.030	·	0.270	**Direct**	SM-41	90%	·	0.030	·	0.270			EPB-205, EPB-206	Counted whole, conservatively: a short that blocks only the release direction has no SG-04 effect. With over-current protection lost (F04-010) a short can drive the motor from the brake state.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-090	New (EPB-121)	10 kOhm DRVOFF pull-up	Open: DRVOFF floats while the MCU pins float	Stop path for an erroneous U14 release command weakened (latent)	RES-0402		0.30	60%	0.180	n/a			·	·	·	·	**Latent**	**LM-01**	90%	·	·	0.018	0.162	F04-020	30.00	EPB-121		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-091	New (EPB-121)	10 kOhm DRVOFF pull-up	Short or drift	Short holds DRVOFF high: the next apply fails (HE-14)	RES-0402		0.30	40%	0.120	n/a			·	·	·	·	**Direct**	**SM-41**	90%	·	0.012	·	0.108				Drift has no effect; counted with the short (conservative). Safe for SG-03.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-092	New (EPB-408)	1 kOhm nSLEEP series resistor	Open: U7 nSLEEP pulled low	U7 asleep: the next apply fails (HE-14)	RES-0402		0.30	60%	0.180	n/a			·	·	·	·	**Direct**	**SM-41**	90%	·	0.018	·	0.162			EPB-408	Safe for SG-03.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-093	New (EPB-408)	1 kOhm nSLEEP series resistor	Short or drift	No SG-04 effect (short: SAFE_OUT1 cannot override nSLEEP; no SG-04 mechanism relies on it)	RES-0402		0.30	40%	0.120	n/a			·	·	·	·	**Safe**			·	·	·	·				Latent for SG-03 (F03-092).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-094	New (EPB-211)	OUTA/OUTB divider resistors	Open, short or drift: terminal readback wrong	Independent terminal and direction monitors blind (latent)	RES-0402	4	1.20	100%	1.200	n/a			·	·	·		**Latent**	**LM-02**	90%	·	·	0.120	1.080	F04-002, F04-014, F04-027, F04-083	1.93	EPB-211, EPB-314	Checked at each commanded operation like the current sense. A short (reads at a rail) is seen at once and is counted with the rest.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-110	U4	TPS62902-Q1	1.25 V core regulated high (half of TI's 'output out of specification' mode)	U14 core overdriven: an erratic release possible (common to both lockstep cores)	U4		12.00	11%	1.320	**Direct**	SM-08	90%	·	**0.132**	·	1.188	**Direct**	SM-08	90%	·	**0.132**	·	1.188			PMC-303, PMC-315	As F03-110. The reset floats the pins: STOP keeps the force.	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F04-111	U4	TPS62902-Q1	High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	U14 core overdriven: an erratic release possible	U4		12.00	10%	1.200	**Direct**	SM-08	90%	·	**0.120**	·	1.080	**Direct**	SM-08	90%	·	**0.120**	·	1.080			PMC-301, PMC-302, PMC-304	As F03-111 (PMC-304 timing, OQ-002).	λ JUDGMENT OQ-010; share JUDGMENT; DC GATED OQ-002
F04-112	U4	TPS62902-Q1	Output low or lost, low-side stuck on, power-FET damage, power-good and enable faults	No SG-04 path (U14 brown-out reset: U7 Hi-Z, force kept; corner loss under SG-02)	U4		12.00	79%	9.480	n/a			·	·	·	·	n/a			·	·	·	·			PMC-306, PMC-307, PMC-308	TI SFFS465A split less the two rows above. Counted n/a rather than Safe.	λ JUDGMENT OQ-010
F04-120	U2	LM68645-Q1	High-side FET short: 12 V rail pulled toward 48V/12V_P	PMIC input overdriven: U14 may act erratically	U2		20.00	10%	2.000	**Direct**	SM-09	90%	·	**0.200**	·	1.800	**Direct**	SM-09	90%	·	**0.200**	·	1.800			PMC-102, BCK-101	The CMPSS window removes 48V/12V_P in about 2 ms (SDAA375); the EPB is then unpowered and self-locked, which is the SG-04 safe state for a held EPB.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-014
F04-121	U2	LM68645-Q1	Output low or lost, regulation faults within the PMIC input range	No SG-04 path	U2		20.00	90%	18.000	n/a			·	·	·	·	n/a			·	·	·	·			PMC-104, PMC-117	Counted n/a rather than Safe.	λ GATED OQ-007; share JUDGMENT
F04-125	U1	LM74930-Q1	Other U1 faults (DGATE drive, current and voltage protection, IMON, pin shorts)	No SG-04 path (48V/12V_P lost: corner loss, SG-02)	U1		14.00	95%	13.300	n/a			·	·	·	·	n/a			·	·	·	·			SUP-209, SUP-305, SUP-311	TI SFFS950 split, less the row below. Counted n/a rather than Safe.	
F04-126	U1	LM74930-Q1	HGATE stuck high: Q1 cannot switch off	Overvoltage cut-off of SM-09 lost (latent)	U1		14.00	5%	0.700	Latent	LM-13	60%	·	·	0.280	0.420	Latent	LM-13	60%	·	·	0.280	0.420	F04-120	2.00	SUP-209, SUP-211	As F03-126.	DC PROVISIONAL OQ-014
F04-127	Q1	SQJA90EP	Drain-source short: the input switch cannot open	Overvoltage cut-off of SM-09 lost (latent)	FET-80V		10.00	40%	4.000	Latent	LM-13	60%	·	·	1.600	2.400	Latent	LM-13	60%	·	·	1.600	2.400	F04-120	2.00	SUP-230		λ JUDGMENT OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-014
F04-128	Q1	SQJA90EP	Open, gate-source short, on-resistance increase	No SG-04 path (48V/12V_P lost: corner loss, SG-02)	FET-80V		10.00	60%	6.000	n/a			·	·	·	·	n/a			·	·	·	·			SUP-212	Counted n/a rather than Safe.	λ JUDGMENT OQ-010; share JUDGMENT (class split)
F04-140	R133, R135	33 Ohm 0402 (SDI, CLK)	Open or drift: SPI-D transfers to U7 and U6 fail	U7 configuration and readback over SPI lost (latent)	RES-0402	2	0.60	90%	0.540	Latent	LM-06	90%	·	·	0.054	0.486	Latent	LM-06	90%	·	·	0.054	0.486	F04-006, F04-022	2.30	EPB-502, EPB-511, EPB-519	Pin control of U7 is unaffected. A U7 left on reset defaults trips OCP at the next apply (SM-41).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-032
F04-141	R133, R135	33 Ohm 0402 (SDI, CLK)	Short	No SG-04 effect (series termination bypassed)	RES-0402	2	0.60	10%	0.060	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F04-150	U8, U10	TCAN1043H-Q1	Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	No SG-04 path (a lost request keeps the hold; a lost status times out at the receiver, which treats the corner as unavailable)	TCAN	2	18.00	98%	17.640	n/a			·	·	·	·	n/a			·	·	·	·			CAN-104, CAN-105, CAN-201, CAN-203	A transceiver cannot forge a CRC-valid release request or status. As F03-150. Counted n/a rather than Safe.	share JUDGMENT
F04-151	U8, U10	TCAN1043H-Q1	Transceiver stays awake when nSTB_CAN goes low (INH held high)	Overvoltage cut-off of SM-09 lost (latent)	TCAN	2	18.00	2%	0.360	Latent	LM-13	60%	·	·	0.144	0.216	Latent	LM-13	60%	·	·	0.144	0.216	F04-120	2.00	CAN-119, CAN-412, CAN-416	As F03-151. It also keeps the corner powered while parked, which exposes the hold to powered release faults longer.	share JUDGMENT; DC PROVISIONAL OQ-014
F04-155	U14	F29P329SM-Q1	CAN transmit path (MCAN, message RAM) corrupts the EPB status (hold or availability reported wrongly)	Report to the other corner and the driver lost (latent)	U14		150.00	1%	1.500	Latent	LM-40	90%	·	·	0.150	1.350	Latent	LM-40	90%	·	·	0.150	1.350	F04-002, F04-008, F04-011, F04-012, F04-014, F04-015, F04-021, F04-	24.51	MCU-508, EPB-510	U14 share taken from 'other'. Partners: the rows whose reaction ends in a report (HAND). A lost message is not latent: the receiver times out and treats the corner as unavailable.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-040
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**103.13 λ**			**0.800**	**5.366**	**4.980**	**79.284**	**105.13 λ**			**0.000**	**4.629**	**5.626**	**88.155**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-05 · Computed (Rev A, provisional)

ASIL B

Avoid erroneous wheel-speed information being used by the braking and stability functions

Safe state: Wheel speed marked invalid; braking functions use the other wheels

FTTI: TBD; provisional 50 ms (ASSUMED) · Hazardous events: HE-18 (S10-QLN-HARA-001 Rev B)

	SPFM · target ≥ 90%	LFM · target ≥ 60%	PMHF (FIT) · item < 100 FIT; corner share open (OQ-046)
As built	**92.79%**	**97.77%**	**4.45**
With actions	**92.85%**	**97.47%**	**4.44**

Key findings

1. SG-05 rests on mechanisms in the brake controller, not in this ECU: cross-wheel plausibility (SM-20), the loss-of-pulse check (SM-23) and the E2E timeout (SM-24). SM-20 sees only deviations above its threshold (ASSUMED max(2 km/h, 5 %) for 20 ms) and is weakest during an ABS intervention, where a low reading looks like a locking wheel. A small speed error from U6, the capture path or the clock is not detected. These checks, their threshold and their timing within the 50 ms FTTI have to be allocated to the brake controller as assumptions of use.

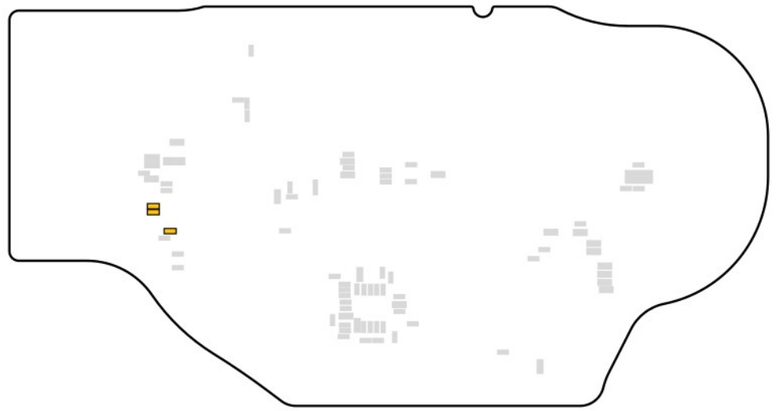
2. The largest residual is lost CAN frames (U8, U10: F05-100, 1.7 FIT), which rests only on the E2E timeout being specified (SM-24, OQ-040). Next comes U6 (about 1.2 FIT), whose FIT and failure-mode split are UNRELEASED assumptions (OQ-008). Its wrong-speed mode (F05-001) is covered by SM-20 alone. The 5 V LDO2 is a common cause for U6 and both CAN transceivers. A lost or shorted 5 V silences the corner, which reveals itself. A 5 V running high relies on the PMIC overvoltage monitor (SM-08), whose LDO2 threshold and reaction are in NVM (OQ-002).

3. The DFMEA actions change little for SG-05. The only hardware action in the chain is the WSSO pull-down (WSS-302), which turns an open WSSO path into a steady low that SM-23 detects. On the ASSUMED data both scenarios reach the recommended ASIL B values: SPFM about 93 %, LFM about 97 %, PMHF about 4.4 FIT. The step that matters is TI's WSS001 FMEDA and a confirmed brake-controller plausibility specification.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Parts that produce, time or carry this corner's wheel speed: the WSS001 decoder (U6), its sensor front end (wire pads J1/J2, D5, R86, R88, C90, C94, C93), its V1P5 capacitor C95, the WSSO path to the MCU (R84, C88) and the U6 SPI readback (R89, and the U7 share of the shared SPI-D bus, EPB-519); the parts of the MCU (U14) that capture, compute and transmit the speed, its clock (Y1, R137); the supplies of U6 (PMIC U3 LDO2 5 V, which also feeds both CAN transceivers, and LDO1 3.3 V; R38 and C92 on the 5 V node; the U2 12 V brown-out band) and the CAN transceivers (U8, U10). The ADC is not in the path (WSSO on AIO203 is used as a digital input). The detection that marks the speed invalid sits mostly in the brake controller (cross-wheel plausibility, loss-of-pulse check, E2E timeout); it is credited as an assumption of use and its own faults belong to that ECU's FMEDA. Faults that collapse a whole rail (12 V, 3.3 V, 5 V decoupling shorts other than C92) silence the corner and are counted under SG-02; PCB shorts between pads are in the PCB analysis. At ASIL B the ISO 26262-5 SPFM (90 %) and LFM (60 %) values are recommended targets, not requirements; they are shown for comparison.

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F05-001	U6	WSS001-Q1	Decoded speed wrong or erratic while pulses continue (current-threshold drift, decoder logic or internal timing reference fault, V1P5 glitches)	Wrong wheel speed reported	U6		15.00	20%	3.000	**Direct**	SM-20	80%	·	**0.600**	·	2.400	**Direct**	SM-20	80%	·	**0.600**	·	2.400			WSS-119, WSS-113	SM-20 detects only deviations above its threshold; an internal timing drift of a few % passes. The DC of SM-20 (0.80) carries that miss. The split of this mode into gross and small errors is unknown (OQ-008).	λ UNRELEASED OQ-008; share UNRELEASED; DC PROVISIONAL OQ-049
F05-002	U6	WSS001-Q1	No speed pulses although the wheel turns (current comparator, decoder, oscillator or WSSO driver fault; VCC5 or VIO pin open)	Wheel speed frozen at zero while moving	U6		15.00	25%	3.750	**Direct**	SM-23	90%	·	**0.375**	·	3.375	**Direct**	SM-23	90%	·	**0.375**	·	3.375			WSS-118, WSS-107, WSS-108		λ UNRELEASED OQ-008; share UNRELEASED; DC PROVISIONAL OQ-049
F05-003	U6	WSS001-Q1	Configuration register or SPI interface fault changes the decoding mode or thresholds; silent reset to defaults	Wrong or missing wheel speed (sensor decoded as the wrong type)	U6		15.00	5%	0.750	**Direct**	SM-22	80%	·	**0.150**	·	0.600	**Direct**	SM-22	80%	·	**0.150**	·	0.600			WSS-121, WSS-122, WSS-313		λ UNRELEASED OQ-008; share UNRELEASED; DC UNRELEASED OQ-008
F05-004	U6	WSS001-Q1	SDO output stuck or readback data wrong	Configuration readback blind (latent)	U6		15.00	5%	0.750	Latent	LM-20	60%	·	·	0.300	0.450	Latent	LM-20	60%	·	·	0.300	0.450	F05-003, F05-050	1.15	WSS-314, EPB-509		λ UNRELEASED OQ-008; share UNRELEASED; DC UNRELEASED OQ-008
F05-005	U6	WSS001-Q1	Internal short from VBAT (12 V) to VIO or VCC5	3.3 V or 5 V rail driven high: U6, U14 and the CAN transceivers overdriven	U6		15.00	5%	0.750	**Direct**	SM-08	90%	·	0.075	·	0.675	**Direct**	SM-08	90%	·	0.075	·	0.675			WSS-110	Common cause with the MCU. The PMIC overvoltage reaction resets U14 and silences the corner, and the brake controller's timeout then marks the speed invalid. Nothing limits the current from 12 V (WSS-110).	λ UNRELEASED OQ-008; share UNRELEASED; DC GATED OQ-002
F05-006	U6	WSS001-Q1	Sensor-supply protection or open/short diagnostics lost, spurious fault flags, other faults that leave the speed correct	No SG-05 effect (a spurious flag marks the speed invalid)	U6		15.00	40%	6.000	Safe			·	·	·	·	Safe			·	·	·	·			WSS-120, WSS-201	The U6 open/short diagnostics are not credited on SG-05 (SM-23 sees the lost pulses without them), so their loss is not latent here; WSS-120 counts it for SG-03.	λ UNRELEASED OQ-008; share UNRELEASED
F05-010	J1	WSP wire pad	Open (crack, lift), permanent or intermittent	Sensor loop open: no pulses, or dropouts	PAD		0.50	70%	0.350	**Direct**	SM-23	90%	·	0.035	·	0.315	**Direct**	SM-23	90%	·	0.035	·	0.315			WSS-203, WSS-204	Dropouts shorter than the SM-23 timeout show as a momentary low speed; only the gradient check of SM-20 sees them, and that is part of the SM-23 miss.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-011	J1	WSP wire pad	Short to an adjacent pad (J20 CAN2L at 4.05 mm) or to the harness	Sensor supply loaded or tied to CAN2L: pulses lost or corrupted	PAD		0.50	30%	0.150	**Direct**	SM-20	80%	·	0.030	·	0.120	**Direct**	SM-20	80%	·	0.030	·	0.120			WSS-202, WSS-218	Corrupted pulses give an erratic speed; a short to ground gives none (then SM-23 also applies).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-012	J2	WSN wire pad	Open (crack, lift), permanent or intermittent	Sensor loop open: no pulses, or dropouts	PAD		0.50	70%	0.350	**Direct**	SM-23	90%	·	0.035	·	0.315	**Direct**	SM-23	90%	·	0.035	·	0.315			WSS-203, WSS-204	As F05-010.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-013	J2	WSN wire pad	Short to J18 (CAN1L, 3.99 mm), J16 (GND, 3.4 mm) or the harness	CAN bit currents decoded as pulses, or sensor return bypassed	PAD		0.50	30%	0.150	**Direct**	SM-20	80%	·	0.030	·	0.120	**Direct**	SM-20	80%	·	0.030	·	0.120			WSS-216, WSS-202, PED-306	CAN traffic decoded as pulses gives a speed far above the other wheels.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-014	D5	ESD2CAN24-Q1	Channel short (IO to GND, or IO1 to IO2)	Sensor supply shorted or sensor bypassed: no pulses	TVS-ESD		1.00	40%	0.400	**Direct**	SM-23	90%	·	0.040	·	0.360	**Direct**	SM-23	90%	·	0.040	·	0.360			WSS-206, WSS-207, WSS-208		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-015	D5	ESD2CAN24-Q1	Leakage or degraded clamp	Sensor current levels shifted: pulses lost or misread without a fault flag	TVS-ESD		1.00	30%	0.300	**Direct**	SM-20	80%	·	0.060	·	0.240	**Direct**	SM-20	80%	·	0.060	·	0.240			WSS-215	Leakage that only shifts the levels slightly may leave a small speed error that SM-20 does not see.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-016	D5	ESD2CAN24-Q1	Open	No SG-05 effect (ESD and surge clamp lost)	TVS-ESD		1.00	30%	0.300	Safe			·	·	·	·	Safe			·	·	·	·			WSS-210, WSS-212	A protection against external stress, not a mechanism against random hardware faults: an ESD event is not a second hardware fault, so the row is not latent.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-020	R86	10 Ohm 0402 (WSP series)	Open	Sensor loop open: no pulses	RES-0402		0.30	60%	0.180	**Direct**	SM-23	90%	·	0.018	·	0.162	**Direct**	SM-23	90%	·	0.018	·	0.162			WSS-209		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F05-021	R86	10 Ohm 0402 (WSP series)	Short or drift	No SG-05 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·			WSS-211	A short removes the current limit between D5 and U6 (a protection, not latent). Drift of a 10 Ohm series part does not move the sensor current levels.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-022	R88	10 Ohm 0402 (WSN series, 1 us filter with C93)	Open	Sensor loop open: no pulses	RES-0402		0.30	60%	0.180	**Direct**	SM-23	90%	·	0.018	·	0.162	**Direct**	SM-23	90%	·	0.018	·	0.162			WSS-209		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-023	R88	10 Ohm 0402 (WSN series, 1 us filter with C93)	Short or drift	No SG-05 effect (input filter weakened: reduced immunity only)	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·			WSS-211, WSS-213		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-024	C90	1 nF 0402 (WSP to GND)	Short	Sensor supply shorted to GND: no pulses	MLCC-0402		0.50	50%	0.250	**Direct**	SM-23	90%	·	0.025	·	0.225	**Direct**	SM-23	90%	·	0.025	·	0.225			WSS-206		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-025	C90	1 nF 0402 (WSP to GND)	Open or capacitance loss	No SG-05 effect (RF filtering lost: reduced immunity)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·			WSS-214		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-026	C94	1 nF 0402 (WSN to GND)	Short	Sensor return bypasses the U6 sense input: no pulses	MLCC-0402		0.50	50%	0.250	**Direct**	SM-23	90%	·	0.025	·	0.225	**Direct**	SM-23	90%	·	0.025	·	0.225			WSS-207		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-027	C94	1 nF 0402 (WSN to GND)	Open or capacitance loss	No SG-05 effect (RF filtering lost: reduced immunity)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·			WSS-214		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-028	C93	0.1 uF 0402 (WSSR to GND)	Short	Sensor return bypasses the U6 sense input: no pulses	MLCC-0402		0.50	50%	0.250	**Direct**	SM-23	90%	·	0.025	·	0.225	**Direct**	SM-23	90%	·	0.025	·	0.225			WSS-207		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-029	C93	0.1 uF 0402 (WSSR to GND)	Open or capacitance loss	No SG-05 effect (1 us filter lost: reduced immunity)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·			WSS-213, WSS-214		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-030	C95	0.33 uF 50 V 0603 (V1P5)	Short	U6 core unsupplied: no pulses	MLCC-0603G		0.50	50%	0.250	**Direct**	SM-23	90%	·	0.025	·	0.225	**Direct**	SM-23	90%	·	0.025	·	0.225			WSS-112		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-031	C95	0.33 uF 50 V 0603 (V1P5)	Open or capacitance loss	V1P5 unstable: U6 core glitches, erratic or wrong speed	MLCC-0603G		0.50	50%	0.250	**Direct**	SM-20	80%	·	0.050	·	0.200	**Direct**	SM-20	80%	·	0.050	·	0.200			WSS-113	Glitches that end in a U6 reset are also caught by SM-22 (reset detection); SM-20 is credited as the weaker of the two.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-032	R84	100 Ohm 0402 (WSSO series)	Open	WSSO input at U14.31 floating: no pulses or random edges	RES-0402		0.30	60%	0.180	**Direct**	SM-20	80%	·	0.036	·	0.144	**Direct**	**SM-23**	90%	·	0.018	·	0.162			WSS-302, WSS-301	As built the input has no pull (WSS-302) and may pick up edges that look like a speed, so only the gross plausibility applies. With the WSSO pull-down the open reads a steady low, which SM-23 detects. U6.8 and U14.31 joint opens behave the same (counted in the U6 and U14 shares).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-033	R84	100 Ohm 0402 (WSSO series)	Short or drift	No SG-05 effect (WSSO filter weakened; eCAP input qualification remains)	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·			WSS-303		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-034	C88	1 nF 0402 (WSSO to GND)	Short	WSSO held low: speed frozen at zero	MLCC-0402		0.50	50%	0.250	**Direct**	SM-23	90%	·	0.025	·	0.225	**Direct**	SM-23	90%	·	0.025	·	0.225			WSS-301		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-035	C88	1 nF 0402 (WSSO to GND)	Open or capacitance loss	No SG-05 effect (WSSO filter lost; eCAP input qualification remains)	MLCC-0402		0.50	50%	0.250	Safe			·	·	·	·	Safe			·	·	·	·			WSS-303		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-036	New (WSS-302)	100 kOhm WSSO pull-down	Open	Defined level on an open WSSO path lost (latent)	RES-0402		0.30	60%	0.180	n/a			·	·	·	·	**Latent**			·	·	0.180	·	F05-032	0.18	WSS-302	Not testable in operation; with it lost, an open WSSO path floats as in scenario A.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-037	New (WSS-302)	100 kOhm WSSO pull-down	Short	WSSO tied to GND: no pulses	RES-0402		0.30	10%	0.030	n/a			·	·	·	·	**Direct**	**SM-23**	90%	·	0.003	·	0.027			WSS-302		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-038	New (WSS-302)	100 kOhm WSSO pull-down	Drift	No SG-05 effect	RES-0402		0.30	30%	0.090	n/a			·	·	·	·	**Safe**			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-050	U7	DRV8263-Q1	SPI pin fault (SDO driven outside its select window, SDI or SCLK loaded) corrupts WSS001 frames on the shared SPI-D	U6 configuration changed	U7		20.00	2%	0.400	**Direct**	SM-22	80%	·	0.080	·	0.320	**Direct**	SM-22	80%	·	0.080	·	0.320			EPB-519, EPB-509, EPB-511, EPB-515	Separate SPI buses for U6 and U7 (EPB-505) would remove this row; that action is not in scenario B.	λ GATED OQ-007; share JUDGMENT; DC UNRELEASED OQ-008
F05-051	U7	DRV8263-Q1	Other U7 functions	Not counted for SG-05	U7		20.00	98%	19.600	n/a			·	·	·	·	n/a			·	·	·	·				Counted under SG-03 and SG-04.	λ GATED OQ-007; share JUDGMENT
F05-052	R89	33 Ohm 0402 (U6 SDO series)	Open	No readback from U6: configuration and reset flag cannot be verified (latent)	RES-0402		0.30	60%	0.180	Latent	LM-20	60%	·	·	0.072	0.108	Latent	LM-20	60%	·	·	0.072	0.108	F05-003, F05-050	1.15	WSS-314		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC UNRELEASED OQ-008
F05-053	R89	33 Ohm 0402 (U6 SDO series)	Short or drift	No SG-05 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·					λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-060	U14	F29P329SM-Q1	CPU, memory or bus fault in the speed computation, the validity flag or the frame content	Wrong wheel speed or validity sent	U14		150.00	3%	4.500	**Direct**	SM-01	99%	·	0.045	·	4.455	**Direct**	SM-01	99%	·	0.045	·	4.455			WSS-301, MCU-508	E2E (SM-24) protects the frame only after it is built; the value relies on the lockstep.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F05-061	U14	F29P329SM-Q1	eCAP, Input X-BAR or AIO203 input path fault: captures missed, doubled or mis-timed	Wrong wheel speed reported	U14		150.00	1%	0.750	**Direct**	SM-20	80%	·	**0.150**	·	0.600	**Direct**	SM-20	80%	·	**0.150**	·	0.600			WSS-304, WSS-301	Outside the lockstep sphere. Gross errors (no captures, doubled or halved rate) are detected by SM-20, or by SM-23 when captures stop; a small timing error is not.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-049
F05-062	U14	F29P329SM-Q1	PLL or clock-divider fault: SYSCLK wrong	Capture timebase wrong: speed scaled	U14		150.00	1%	0.750	**Direct**	SM-21	90%	·	0.075	·	0.675	**Direct**	SM-21	90%	·	0.075	·	0.675			MCU-203, MCU-204	The DCC compares PLLRAWCLK with INTOSC; errors within the INTOSC tolerance (about 3 %) are not seen.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F05-063	U14	F29P329SM-Q1	MCAN module or message-RAM fault: wheel-speed frames lost, frozen or corrupted	Wrong or stale wheel speed at the brake controller	U14		150.00	1%	1.500	**Direct**	SM-24	90%	·	**0.150**	·	1.350	**Direct**	SM-24	90%	·	**0.150**	·	1.350			MCU-508		λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-040
F05-064	U14	F29P329SM-Q1	Lockstep comparator, ECC or error-signal module fault	MCU self-monitoring blind (latent)	U14		150.00	5%	7.500	Latent	LM-04	90%	·	·	0.750	6.750	Latent	LM-04	90%	·	·	0.750	6.750	F05-060	4.50	MCU tab		λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F05-065	U14	F29P329SM-Q1	Missing-clock detection or DCC fault, or their configuration lost	Clock monitoring blind (latent)	U14		150.00	1%	0.750	Latent	LM-04	90%	·	·	0.075	0.675	Latent	LM-04	90%	·	·	0.075	0.675	F05-062, F05-070, F05-073	2.82	MCU-204	LM-04 must include the start-up test of the MCD and DCC that MCU-204 asks for.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F05-066	U14	F29P329SM-Q1	Other MCU functions (BLDC and EPB control, other peripherals)	Not counted for SG-05	U14		150.00	90%	134.250	n/a			·	·	·	·	n/a			·	·	·	·				Excluded rather than counted as safe, as on SG-03.	λ GATED OQ-007; share JUDGMENT
F05-070	Y1	CDC6C-Q1	No output clock (30 % of die and the package failures), or frequency error beyond the DCC window (about 3 %)	Capture timebase lost or wrong: speed scaled or frozen	Y1		3.00	63%	1.890	**Direct**	SM-21	90%	·	**0.189**	·	1.701	**Direct**	SM-21	90%	·	**0.189**	·	1.701			MCU-201, MCU-203	Shares from TI SFFS685: no clock 0.6 FIT die + 1 FIT package, and half of the wrong-frequency mode (0.3 FIT) taken as beyond 3 %. The half-and-half split of the wrong-frequency mode is sev10's judgment.	DC GATED OQ-007
F05-071	Y1	CDC6C-Q1	Frequency error between the CAN bit-timing tolerance (about 1 %, ASSUMED) and the DCC window	Speed scaled by the error; this node's CAN frames fail	Y1		3.00	5%	0.150	**Direct**	SM-24	90%	·	0.015	·	0.135	**Direct**	SM-24	90%	·	0.015	·	0.135			MCU-203	The MCAN bit clock comes from the same X1, so an error beyond the bit-timing tolerance puts the node error-passive or bus-off and the frames stop. The tolerance depends on the bit timing (OQ-039).	DC PROVISIONAL OQ-040

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F05-072	Y1	CDC6C-Q1	Frequency error within about 1 %, jitter or duty-cycle degradation	No SG-05 effect (speed error below 1 %)	Y1		3.00	32%	0.960	Safe			·	·	·	·	Safe			·	·	·	·			MCU-203	Not detected by any mechanism. Classified safe on the assumption that the ABS/ESC tolerates a 1 % error at one wheel (it must handle larger tyre-radius differences anyway); to be confirmed with the brake-controller supplier (proposed question). Nanosecond jitter has no effect on millisecond pulse periods.	
F05-073	R137	33 Ohm 0402 (X1 series)	Open	Clock lost at X1: capture timebase lost	RES-0402		0.30	60%	0.180	**Direct**	SM-21	90%	·	0.018	·	0.162	**Direct**	SM-21	90%	·	0.018	·	0.162			MCU-202		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC GATED OQ-007
F05-074	R137	33 Ohm 0402 (X1 series)	Short or drift	No SG-05 effect	RES-0402		0.30	40%	0.120	Safe			·	·	·	·	Safe			·	·	·	·			MCU-202		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F05-080	U3	TPS653860-Q1	LDO2 (5 V) regulates high or its pass element shorts toward VCC_6V0	U6 VCC5 overstressed: decoding lost or erratic while CAN still transmits	U3		40.00	1%	0.400	**Direct**	SM-08	90%	·	0.040	·	0.360	**Direct**	SM-08	90%	·	0.040	·	0.360			WSS-111, PMC-207	Common cause with U8 and U10. SM-08 as defined covers LDO1 and the core only; it must be extended to the LDO2 overvoltage (proposed note). The reaction resets U14 and the corner goes silent, which the brake controller's timeout marks invalid.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F05-081	U3	TPS653860-Q1	LDO2 (5 V) low or drifting, below the U6 minimum while the CAN transceivers still work	U6 decodes erratically or stops	U3		40.00	1%	0.400	**Direct**	SM-20	80%	·	0.080	·	0.320	**Direct**	SM-20	80%	·	0.080	·	0.320			WSS-107, PMC-207	The LDO2 undervoltage reaction is set in NVM and may be a flag only (OQ-002), so the credit is on the effect (SM-20; SM-23 when the pulses stop).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-049
F05-082	U3	TPS653860-Q1	LDO1 (3.3 V) regulates high	U6 VIO, Y1 and U14 I/O overdriven: WSSO and captures unreliable	U3		40.00	1%	0.400	**Direct**	SM-08	90%	·	0.040	·	0.360	**Direct**	SM-08	90%	·	0.040	·	0.360			MCU-209, WSS-109, PMC-206	Same failure mode as F03-034; the LDO1 monitor shares the die with the regulator (OQ-002).	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-002
F05-083	U3	TPS653860-Q1	Rail monitors (LDO1, LDO2 overvoltage), watchdog, error monitor or NRST fail to act	Supply and MCU-error reactions lost (latent)	U3		40.00	2%	0.800	Latent	LM-05	90%	·	·	0.080	0.720	Latent	LM-05	90%	·	·	0.080	0.720	F05-005, F05-080, F05-082, F05-060	6.05	PMC-312, PMC-404, PMC-405	Partner F05-060: the lockstep reaction (SM-01) runs through the PMIC reset.	λ GATED OQ-007; share JUDGMENT; DC GATED OQ-007
F05-084	U3	TPS653860-Q1	Other PMIC functions (other regulators, rail loss, pedal supplies)	Not counted for SG-05	U3		40.00	95%	38.000	n/a			·	·	·	·	n/a			·	·	·	·				Loss of a rail resets U14 or silences the corner (SG-02).	λ GATED OQ-007; share JUDGMENT
F05-090	R38	0 Ohm 0402 (LDO2 output link)	Open	5 V lost at U6, U8 and U10 together; LDO2 sees no load and its monitor stays quiet	RES-0R		0.10	100%	0.100	**Direct**	SM-24	90%	·	0.010	·	0.090	**Direct**	SM-24	90%	·	0.010	·	0.090			PMC-207	Common cause (MC-03 at vehicle level). U6 stops and both CAN channels go silent, so no wrong value is sent; the brake controller's timeout marks the corner invalid.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-040
F05-091	C92	0.1 uF 0402 (U6 VCC5)	Short	5 V rail shorted at U6: U6 and both CAN channels lost	MLCC-0402		0.50	50%	0.250	**Direct**	SM-24	90%	·	0.025	·	0.225	**Direct**	SM-24	90%	·	0.025	·	0.225			WSS-106, CAN-214	Counted here as the 5 V short local to U6; the other 5 V decoupling shorts behave the same and are counted under SG-02.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-040
F05-092	C92	0.1 uF 0402 (U6 VCC5)	Open or capacitance loss	U6 decodes false or missing pulses under supply disturbance	MLCC-0402		0.50	50%	0.250	**Direct**	SM-20	80%	·	0.050	·	0.200	**Direct**	SM-20	80%	·	0.050	·	0.200			WSS-114		λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC PROVISIONAL OQ-049
F05-093	U2	LM68645-Q1	12 V output low, in a band where U3 and U14 run but U6 VBAT is below its minimum	U6 unsupplied: no pulses	U2		20.00	5%	1.000	**Direct**	SM-23	90%	·	**0.100**	·	0.900	**Direct**	SM-23	90%	·	**0.100**	·	0.900			WSS-103, BCK-408	The U6 VBAT minimum is unknown (OQ-008).	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-049
F05-094	U2	LM68645-Q1	Other U2 faults (output lost, 12 V overvoltage)	Not counted for SG-05	U2		20.00	95%	19.000	n/a			·	·	·	·	n/a			·	·	·	·				A lost 12 V silences the corner (SG-02); 12 V overvoltage is counted under SG-01 and SG-03 (SM-09).	λ GATED OQ-007; share JUDGMENT
F05-100	U8, U10	TCAN1043H-Q1	Receiver, transmitter, stuck in sleep, bus dominant or pin short	Wheel-speed frames lost on that channel	TCAN	2	18.00	95%	17.100	**Direct**	SM-24	90%	·	**1.710**	·	15.390	**Direct**	SM-24	90%	·	**1.710**	·	15.390			CAN-112, CAN-214	TI SLLA525A split. A receiver fault makes the node see its own frames as errors and go bus-off. Which channels carry the speed is open (OQ-039); both are counted. CAN CRC and E2E stop a corrupted frame from being used.	DC PROVISIONAL OQ-040
F05-101	U8, U10	TCAN1043H-Q1	False fault report	No SG-05 effect	TCAN	2	18.00	5%	0.900	Safe			·	·	·	·	Safe			·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**61.75 λ**			**0.000**	**4.454**	**1.277**	**46.259**	**62.05 λ**			**0.000**	**4.439**	**1.457**	**46.304**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

SG-06 · No metric targets (ASIL A)

ASIL A

Provide parking-brake deceleration when the driver requests it and service braking is unavailable

Safe state: Not applicable (availability goal)

FTTI: TBD · Hazardous events: HE-16 (S10-QLN-HARA-001 Rev B)

What the computation would cover

Elements	EPB apply path (U7, Q11, U14) when service braking is unavailable
Dominant parts	Not applicable: no hardware metric targets at ASIL A
Mechanisms	Covered by the DFMEA and the safety requirements
Waits for	None: ISO 26262-5 sets SPFM, LFM and PMHF targets from ASIL B upward
Why	ISO 26262-5 sets SPFM, LFM and PMHF targets from ASIL B upward. At ASIL A the hardware is covered by the DFMEA and the safety requirements; the tab is kept so the workbook covers every goal.

Not computed in this example package. In a customer engagement, SG-06 would be analysed in full with the same method, row structure and checks as the computed goals: every failure mode on the goal's path, classified per scenario, with its mechanisms, assumptions and open questions. At ASIL A, ISO 26262-5 sets no hardware metric targets; the goal would still be covered through the DFMEA and the safety requirements. For worked results, see SG-01, SG-02, SG-03, SG-04, SG-05 and SG-07.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

SG-07 · Computed (Rev A, provisional)

ASIL B

Avoid a thermal event (smoke, fire) of the corner ECU

Safe state: Energy removed from the faulty circuit; corner reported unavailable; driver warned to stop

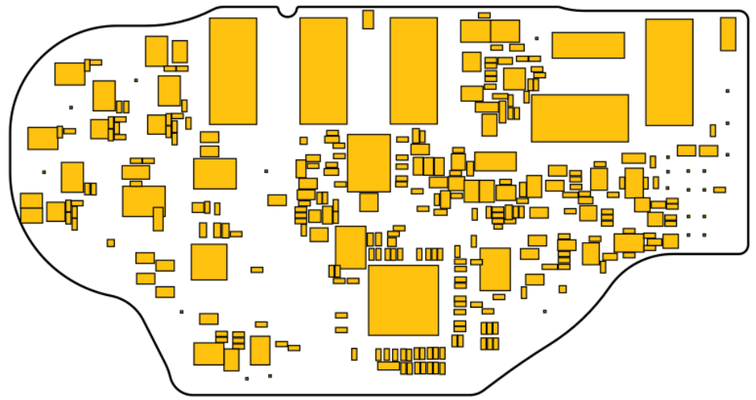
FTTI: TBD; U1 acts in microseconds to 1 ms, the IMON check needs the time to ignition to exceed its period plus debounce (ASSUMED, OQ-044) · H

	SPFM · target ≥ 90%	LFM · target ≥ 60%	PMHF (FIT) · item < 100 FIT; corner share open (OQ-046)
As built	60.29%	87.22%	28.45
With actions	75.96%	87.23%	13.86

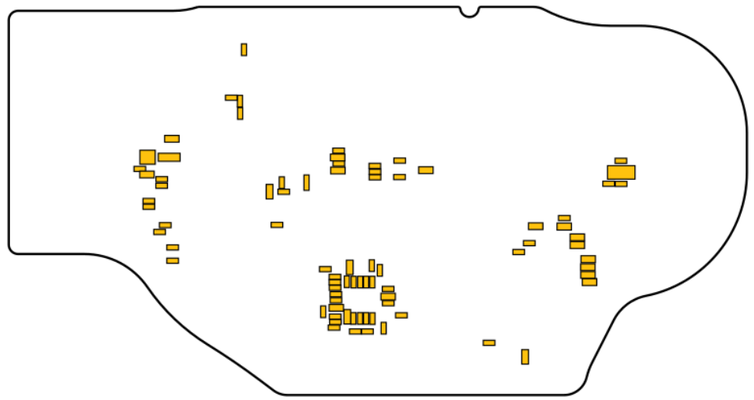
Key findings

1. As built, nothing on VerB sees a fault that draws less than the U1 breaker band (18-27 A): the resistive half of every 48 V and 12 V capacitor short, every CAF path, a hot power-pad joint and a leaky input TVS are single-point faults, and the whole input side ahead of R7 is protected only by the vehicle fuse for hard shorts. The U1 short-circuit comparator and breaker are the only mechanism, and their loss (U1 SCP/OCP, the set network, R7) is latent with no test. SPFM as built is about 60 % against the 90 % recommended; LFM (about 87 %) meets 60 % only because the latent faults are small next to the covered hard shorts. PMHF about 28 FIT for one corner, so four corners alone exceed the 100 FIT item value (OQ-046).
2. With the actions the gap narrows but stays. The IMON supply-current check (PCB-202, SUP-314) sees only the high-power end (above about 3 A), and the actions leave CAF ahead of R7 and on the phases, hot pad joints and 12 V rail shorts without any mechanism. Closing it needs a fail-safe element rather than more software: fail-open (floating-electrode) bus MLCCs or an eFuse below the U1 band (PCB-202), a current limit on the 12 V rail, an idle-current trip on the EPB branch through Q11 (an extension of EPB-423), and CAF-resistant laminate with 0.5 mm inner spacing (PCB-302, PCB-303). SPFM with the actions is about 76 %, PMHF about 14 FIT.
3. Several thermal chains are systematic and sit outside these metrics: D1 (SMBJ51CA) conducts continuously near 60 V (SUP-101); as built Q11 runs as a source follower and dissipates tens of watts in every EPB actuation (EPB-402, R58); C27 and C31-C33 are 85 C parts at a 105 C board (BCK-409); Q1 exceeds its SOA at every start (SUP-201). Each must be closed by design before the random-fault metrics mean anything.

TOP



BOTTOM (mirrored)



Board drawing: sev10, from TI Gerber and IPC-356 data. Yellow = parts of the circuit behind this goal.

Scope: Parts on the energy-carrying nets whose faults can become a sustained heat source: the 48 V input side ahead of the U1 current sense R7 (C7-C10 incl. the input electrolytic C8, TVS D1, wire pads 13/34), the 48V/12V_P bus downstream of R7 (the 1210, 0603 and 1206 bus MLCCs, the aluminium bulk C28, C60, C73, C74, the U2 input), the EPB branch 48V/12V_BDC (C96, C97, U7 VM), the 12 V rail fed by U2 (its capacitors, U2 and its feedback), the inverter phases (Q4, Q5, Q7-Q10, pads J7-J9) and the inner-layer CAF paths of these nets. The elements of the mechanisms that remove the energy are counted for their latent faults: U1, its OCP/SCP set network and R7, Q1/Q2, the INH path (U8/U10, INH network) and the VMON divider of the 12 V cut-off. Left out, with the reason: logic and low-energy rails (3.3 V, 5 V, 1.25 V; PMIC-limited to well under 1 A), the small-signal branches that fuse open at a few amps (VSUP dropper D3/D11/C16, U1 VS clamp, Q6 and its 22 kOhm bias network, whose 58-66 V overstress of EPB-405 is limited by the U5 charge pump), and the EPB output side (OUTA/OUTB copper, J5/J6, U7 OCP and thermal shutdown): the self-locking spindle needs current only for about a second per actuation, so a resistive fault there cannot accumulate heat, and U7 OCP ends a hard one. Q11 is a series switch with no thermal path of its own. Surface leakage and dendrites across bare 48 V gaps (PCB-101, the Q11.1-C96.1 pads of EPB-423, SUP-230) need a humidity event acting on the whole board: they go to the dependent-failure analysis with the coating decision (OQ-030), as on SG-01; a solder bridge there is a production defect (PFMEA). Faults that remove supply or only open a path are n/a, not Safe. Systematic thermal chains (D1 conducting at 60 V, Q11 in linear operation as built, 25 V capacitors at 105 C, the R22 variant, electrolytic wear-out) are design deficiencies, not random faults: they are listed in the findings and the dependent-failure note, not in the metrics. At ASIL B the ISO 26262-5 SPFM (90 %) and LFM (60 %) values are recommended targets, not requirements; the ASIL itself awaits confirmation (OQ-044).

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F07-001	C8	330 uF 100 V aluminium (EMVE)	Internal short, hard (half of the 20 % short mode)	48V/12V_IN shorted ahead of R7: battery current through J3, L1 and the short	ALU-100V		3.00	10%	0.300	**Direct**	SM-73	60%	·	**0.120**	·	0.180	**Direct**	SM-73	60%	·	**0.120**	·	0.180			SUP-104, PCB-302	U1 senses only R7, downstream of this fault. The vehicle fuse at J3/J4 clears a hard short (rating unknown, OQ-025).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC NO-CLIENT-DATA OQ-025
F07-002	C8	330 uF 100 V aluminium (EMVE)	Internal short, resistive (half of the 20 % short mode)	Sustained heat in C8 below the vehicle fuse rating: smoke, venting, charring	ALU-100V		3.00	10%	0.300	**Direct**			**0.300**	·	·	·	**Direct**			**0.300**	·	·	·			SUP-104, PCB-302	No on-board limit ahead of R7. The SUP-104 action (bulk moved behind the reverse-blocking FET) targets reverse polarity and is not credited here.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-003	C8	330 uF 100 V aluminium (EMVE)	Venting after internal heating (ESR rise with ripple)	Hot, flammable electrolyte vapour released onto the board (smoke)	ALU-100V		3.00	10%	0.300	**Direct**			**0.300**	·	·	·	**Direct**			**0.300**	·	·	·			BLD-404, SUP-104	Nothing detects rising ESR on the input side. Wear-out beyond the constant rate is a design item (BLD-404, OQ-010).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-004	C8	330 uF 100 V aluminium (EMVE)	Open, capacitance loss or ESR rise without venting	No SG-07 effect (input filtering reduced)	ALU-100V		3.00	70%	2.100	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-005	C7, C9, C10	0.1 uF 100 V X8L 0603 soft termination	Short, hard	Input net (NetC7_2 or 48V/12V_IN_FILTERED) shorted ahead of R7	MLCC-0603	3	2.40	25%	0.600	**Direct**	SM-73	60%	·	**0.240**	·	0.360	**Direct**	SM-73	60%	·	**0.240**	·	0.360			SUP-220, SUP-108, PCB-507	U1 SCP/OCP see nothing (SUP-220). The SUP-220 action asks for a per-corner fuse sized for this short (A-09).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC NO-CLIENT-DATA OQ-025
F07-006	C7, C9, C10	0.1 uF 100 V X8L 0603 soft termination	Short, resistive	Sustained heat at an 0603 ahead of R7, no on-board limit	MLCC-0603	3	2.40	25%	0.600	**Direct**			**0.600**	·	·	·	**Direct**			**0.600**	·	·	·			SUP-220, SUP-108	SUP-220: 'a resistive short (cracked C7) is not detected at all and burns'. C9 sits on the bottom side (PCB-507).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-007	C7, C9, C10	0.1 uF 100 V X8L 0603 soft termination	Open or capacitance loss	No SG-07 effect	MLCC-0603	3	2.40	50%	1.200	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-008	D1	SMBJ51CA TVS (SMB)	Short (fused junction)	48V/12V_IN shorted at the pad ahead of U1	TVS-SMB		2.00	40%	0.800	**Direct**	SM-73	60%	·	**0.320**	·	0.480	**Direct**	SM-73	60%	·	**0.320**	·	0.480			SUP-101	A failed TVS junction is low-ohmic: hard. Continuous conduction at 57-60 V (VBR min 56.7 V) is a design deficiency (SUP-101, OQ-017), not counted here.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split); DC NO-CLIENT-DATA OQ-025
F07-009	D1	SMBJ51CA TVS (SMB)	Leakage or degraded clamp	Leakage near VBR at 54-60 V runs away thermally in the SMB package	TVS-SMB		2.00	30%	0.600	**Direct**			**0.600**	·	·	·	**Direct**			**0.600**	·	·	·			SUP-101	Nothing on the board measures the input-side current. The SUP-101 action (higher VBR, local fusible element) would make this row Safe once specified.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)
F07-010	D1	SMBJ51CA TVS (SMB)	Open	No SG-07 effect (surge clamp lost: an external surge is a dependent failure)	TVS-SMB		2.00	30%	0.600	n/a			·	·	·	·	n/a			·	·	·	·			SUP-105	No thermal path from a random fault.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)
F07-011	J3, J4	Battery and ground wire pads (hand-soldered slots)	Joint degrades to high resistance and heats (half of the 70 % open mode)	Pad and wire overheat at the full ECU current; creep, reflow, solder or strand dropped toward the next pad	PAD	2	1.00	35%	0.350	**Direct**			**0.350**	·	·	·	**Direct**			**0.350**	·	·	·			PCB-502, PCB-501	J3/J4 carry the whole supply current whenever the ECU is awake. The supply-path resistance estimate of PCB-502 is only a 'requires SW' note, not an action; the connector action (OQ-004) changes the part but keeps the mode.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-012	J3, J4	Battery and ground wire pads (hand-soldered slots)	Clean open (crack, lift)	No SG-07 effect (supply or ground lost)	PAD	2	1.00	35%	0.350	n/a			·	·	·	·	n/a			·	·	·	·			SUP-113	No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-013	J3, J4	Battery and ground wire pads (hand-soldered slots)	Short between J3 and J4 or to the harness	48V/12V_IN shorted to GND ahead of R7	PAD	2	1.00	30%	0.300	**Direct**	SM-73	60%	·	**0.120**	·	0.180	**Direct**	SM-73	60%	·	**0.120**	·	0.180			PCB-501, PCB-502	A pad bridge or stray strand is metallic: hard.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC NO-CLIENT-DATA OQ-025
F07-020	U1	LM74930-Q1	Short-circuit comparator fails to act (TI SCP 5 %)	Hard shorts downstream of R7 left to the 1 ms breaker (latent)	U1		14.00	5%	0.700	Latent			·	·	0.700	·	Latent			·	·	0.700	·	F07-040, F07-043, F07-046, F07-050, F07-053, F07-056,	34.35	SUP-314	No test of the comparators exists (SUP-314: 'none on VerB'); a bench test of a good board runs with the protection idle. Full λ latent.	
F07-021	U1	LM74930-Q1	Overcurrent circuit breaker fails to act (TI OCP 6 %)	Shorts in the 18-34 A band no longer removed (latent)	U1		14.00	6%	0.840	Latent			·	·	0.840	·	Latent			·	·	0.840	·	F07-040, F07-043, F07-046, F07-050, F07-	34.35	SUP-314	As F07-020. The IMON overload check that SUP-314 asks for is not an action, so not credited.	
F07-022	U1	LM74930-Q1	HGATE stuck high (TI 5 %): Q1 cannot be turned off	Reaction of SM-70, SM-09 and SM-71 lost (latent)	U1		14.00	5%	0.700	Latent	LM-13	60%	·	·	0.280	0.420	Latent	LM-13	60%	·	·	0.280	0.420	F07-040, F07-043, F07-046, F07-050, F07-	42.01	SUP-209, SUP-211, SUP-404	Same row as F01-110. The key-off cut-off test (LM-13) sees Q1 still on.	DC PROVISIONAL OQ-014
F07-023	U1	LM74930-Q1	IMON output wrong (TI 5 %)	Supply-current check blind (latent)	U1		14.00	5%	0.700	n/a			·	·	·	·	**Latent**	**LM-70**	90%	·	·	0.070	0.630	F07-044, F07-047, F07-054, F07-057, F07-061, F07-091	5.45	SUP-322, SUP-325, PCB-202	As built IMON serves no SG-07 mechanism: n/a. With the actions it is the input of SM-71; a stuck-low IMON reads as a quiet bus at idle, so only the actuation plausibility of LM-70 finds it.	DC PROVISIONAL OQ-032

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F07-024	U1	LM74930-Q1	Pin-to-pin short (TI 5 %)	An input-side pin (VS, A, CS+) joined to GND or a neighbour ahead of R7: package heats until a bond wire fuses or the vehicle fuse clears	U1		14.00	5%	0.700	**Direct**			**0.700**	·	·	·	**Direct**			**0.700**	·	·	·			SUP-220, PCB-101	Counted whole and uncovered (conservative): TI does not say which pairs join 48 V to GND, and SUP-220 names U1.2, U1.15, U1.24 to GND as unseen by the breaker. The 0.25 mm U1.13/U1.14 gap at 59-65 V is a PCB item (PCB-101).	
F07-025	U1	LM74930-Q1	DGATE modes, HGATE out of spec or stuck low, UV/OV (TI 40 + 26 + 8 %)	No SG-07 effect (48V/12V_P lost, or reverse or surge protection lost)	U1		14.00	74%	10.360	n/a			·	·	·	·	n/a			·	·	·	·			SUP-305, SUP-311, SUP-401	TI SFFS950 split. No thermal path; an external surge is a dependent failure.	
F07-026	R7, R11, C14, R20, C19, R21	U1 sense and OCP/SCP set network	R11 open, C14 short (CS+ = CS-), R20 or R21 short, C19 short, R7 drifting low	OCP or SCP disabled or its trip level raised (latent)	U1-NET		2.90	38%	1.102	Latent			·	·	1.102	·	Latent			·	·	1.102	·	F07-040, F07-043, F07-046, F07-050, F07-053. F07-056.	34.35	SUP-314	Split in the U1-NET key. R11 is an ATC 504L without an AEC-Q200 statement (OQ-018). No test; full λ latent.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-027	R7, R11, C14, R20, C19, R21	U1 sense and OCP/SCP set network	Other modes (R7 open or drifting high, R11 short, filter or timer shortened, R21 open)	No SG-07 effect (false trip, supply lost, or auto-retry instead of latch-off)	U1-NET		2.90	62%	1.798	n/a			·	·	·	·	n/a			·	·	·	·			SUP-315	R21 open turns latch-off into auto-retry: each retry into a hard short is bounded by the SCP delay, so no sustained heat (JUDGMENT).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-028	Q1, Q2	SQJA90EP	Q1 drain-source short (40 % of Q1)	U1 can no longer remove the supply: reaction of SM-70, SM-09 and SM-71 lost (latent)	FET-80V	2	20.00	20%	4.000	Latent	LM-13	60%	·	·	1.600	2.400	Latent	LM-13	60%	·	·	1.600	2.400	F07-040, F07-043, F07-046, F07-050, F07-053. F07-056.	42.01	SUP-208, SUP-230	Share of the Q1/Q2 pair, as F01-113. Q1 SOA overstress at start-up (SUP-201) raises this mode as built; it is a design item.	λ JUDGMENT OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F07-029	Q1, Q2	SQJA90EP	Q1 other modes; any Q2 mode	No SG-07 effect (supply lost or lossy, reverse blocking lost)	FET-80V	2	20.00	80%	16.000	n/a			·	·	·	·	n/a			·	·	·	·			SUP-212	On-resistance increase is bounded by the load current; the FET ends open or shorted before the laminate reaches Td (JUDGMENT).	λ JUDGMENT OQ-010; share JUDGMENT
F07-030	U8, U10	TCAN1043H-Q1	Transceiver stays awake when nSTB_CAN goes low (INH held high)	Reaction of SM-09 and SM-71 lost (latent)	TCAN	2	18.00	2%	0.360	Latent	LM-13	60%	·	·	0.144	0.216	Latent	LM-13	60%	·	·	0.144	0.216	F07-062, F07-065, F07-044, F07-047, F07-	7.66	CAN-119, CAN-408, CAN-412	Same share as F01-115. SM-70 acts inside U1 and does not need INH.	share JUDGMENT; DC PROVISIONAL OQ-014
F07-031	U8, U10	TCAN1043H-Q1	Other transceiver faults	No SG-07 effect	TCAN	2	18.00	98%	17.640	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	share JUDGMENT
F07-032	INH network	D6, D7, R102, R112, R156, R19, R26, R36	R156 open: INH_CAN floats instead of going low	Reaction of SM-09 and SM-71 lost (latent)	INH-NET		3.80	5%	0.190	Latent	LM-13	60%	·	·	0.076	0.114	Latent	LM-13	60%	·	·	0.076	0.114	F07-062, F07-065, F07-044, F07-047, F07-054. F07-057.	7.66	CAN-409	As F01-117.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F07-033	INH network	D6, D7, R102, R112, R156, R19, R26, R36	Other faults	No SG-07 effect	INH-NET		3.80	95%	3.610	n/a			·	·	·	·	n/a			·	·	·	·			SUP-405	No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-034	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Drift: VMON reads 12 V low	12 V overvoltage cut-off acts late or not at all (latent)	RES-0402	2	0.60	30%	0.180	Latent			·	·	0.180	·	Latent			·	·	0.180	·	F07-062, F07-065	2.21	MCU-306, BCK-206	As F01-104: the CMPSS DAC-code test of LM-13 does not test the divider scale.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-035	R130, R131	10 kOhm, 1 kOhm 0402 (VMON divider)	Open or short	No SG-07 effect (CMPSS window trips, corner off)	RES-0402	2	0.60	70%	0.420	n/a			·	·	·	·	n/a			·	·	·	·			MCU-306	No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-040	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs as built (7 x GRM 1210 general grade, 2 x 0603, 1 x 1206)	Crack or dielectric short, hard	48V/12V_P shorted to GND above the U1 band	BUS-MLCC		16.60	25%	4.150	**Direct**	SM-70	90%	·	**0.415**	·	3.735	n/a			·	·	·	·			SUP-417, BCK-103, BLD-401, BLD-402, PCB-201,	U1 SCP (3.5-5.5 us) or breaker, then latch-off (R21). Replaced by the actions (row F07-043).	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC JUDGMENT OQ-028
F07-041	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs as built (7 x GRM 1210 general grade, 2 x 0603, 1 x 1206)	Crack short, resistive (about 3-300 Ohm)	10 W to 1 kW in one capacitor site below the U1 band: charring, spread to adjacent nets, smoke or fire	BUS-MLCC		16.60	25%	4.150	**Direct**			**4.150**	·	·	·	n/a			·	·	·	·			PCB-202, SUP-417, BCK-103, BLD-401	The rated FE-29 chain. Murata excludes the GRM series from this use and asks for a fail-safe such as a fuse (p.24); VerB has none below 18 A.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT
F07-042	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs as built (7 x GRM 1210 general grade, 2 x 0603, 1 x 1206)	Open or capacitance loss	No SG-07 effect (decoupling reduced)	BUS-MLCC		16.60	50%	8.300	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)
F07-043	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs with actions (1210 AEC-Q200 soft termination, moved from the edge)	Crack or dielectric short, hard	48V/12V_P shorted to GND above the U1 band	BUS-MLCC-B		9.60	25%	2.400	n/a			·	·	·	·	**Direct**	**SM-70**	90%	·	**0.240**	·	2.160			SUP-417, BCK-103, BLD-401, PCB-201	Scenario B takes the soft-termination option of the actions. Fail-open (floating-electrode) parts, the other option, would move most of the short mode to open.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC JUDGMENT OQ-028
F07-044	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs with actions (1210 AEC-Q200 soft termination, moved from the edge)	Crack short, resistive (about 3-300 Ohm)	10 W to 1 kW in one capacitor site below the U1 band	BUS-MLCC-B		9.60	25%	2.400	n/a			·	·	·	·	**Direct**	**SM-71**	60%	·	**0.960**	·	1.440			PCB-202	SM-71 sees the part above about 3 A (160 W); below that nothing acts.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC PROVISIONAL OQ-044
F07-045	C5, C6, C21, C22, C61, C75, C76, C23, C24, C68	Bus MLCCs with actions (1210 AEC-Q200 soft termination, moved from the edge)	Open or capacitance loss	No SG-07 effect	BUS-MLCC-B		9.60	50%	4.800	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)
F07-046	C28, C60, C73, C74	100/330 uF 100 V aluminium (EMVE)	Internal short, hard (half of the 20 % short mode)	48V/12V_P shorted to GND above the U1 band	ALU-100V	4	12.00	10%	1.200	**Direct**	SM-70	90%	·	**0.120**	·	1.080	**Direct**	SM-70	90%	·	**0.120**	·	1.080			BLD-403, BCK-103		λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC JUDGMENT OQ-028
F07-047	C28, C60, C73, C74	100/330 uF 100 V aluminium (EMVE)	Internal short, resistive	Sustained heat in the can below the U1 band: venting, charring	ALU-100V	4	12.00	10%	1.200	**Direct**			**1.200**	·	·	·	**Direct**	**SM-71**	60%	·	**0.480**	·	0.720			BLD-403		λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-044
F07-048	C28, C60, C73, C74	100/330 uF 100 V aluminium (EMVE)	Venting after internal heating (ESR rise with ripple)	Hot, flammable electrolyte vapour on the board (smoke); conductive residue on adjacent pads	ALU-100V	4	12.00	10%	1.200	**Direct**			**1.200**	·	·	·	**Direct**			**1.200**	·	·	·			BLD-403, BLD-404	No detection of venting (BLD-403). BLD-404's ESR estimate is a 'requires SW' note, not an action; its action is a life calculation (prevention).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-049	C28, C60, C73, C74	100/330 uF 100 V aluminium (EMVE)	Open, capacitance loss or ESR rise without venting	No SG-07 effect (bus ripple up: SG-02)	ALU-100V	4	12.00	70%	8.400	n/a			·	·	·	·	n/a			·	·	·	·			BLD-404	No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-050	C96, C97	EPB bulk as built (C96 GRM 1210 general grade, C97 0603 soft termination)	Crack or dielectric short, hard	48V/12V_BDC shorted: bus pulled into the U1 SCP through Q11	BDC-MLCC		2.80	25%	0.700	**Direct**	SM-70	90%	·	0.070	·	0.630	n/a			·	·	·	·			EPB-201, EPB-423	U1 latches the whole corner off. With 48V/12V_BDC at 0 V, Q11 VGS reaches 48-66 V and its gate ruptures (EPB-417): no thermal consequence, U1 has already removed the energy.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC JUDGMENT OQ-028
F07-051	C96, C97	EPB bulk as built (C96 GRM 1210 general grade, C97 0603 soft termination)	Crack short, resistive (EPB-201: 2-20 A)	Up to about 1 kW at C96 or C97 below the U1 band: charring spreads to other nets	BDC-MLCC		2.80	25%	0.700	**Direct**			**0.700**	·	·	·	n/a			·	·	·	·			EPB-201, PCB-202	Q11 has no current sense and, with R58 fitted, cannot open. The Q11.1-C96.1 pad bridge of EPB-423 ends the same way; as a humidity-driven surface path it is in the dependent-failure analysis (scope).	λ NO-CLIENT-DATA OQ-018; share JUDGMENT
F07-052	C96, C97	EPB bulk as built (C96 GRM 1210 general grade, C97 0603 soft termination)	Open or capacitance loss	No SG-07 effect (U7 VM ripple)	BDC-MLCC		2.80	50%	1.400	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)
F07-053	C96, C97	EPB bulk with actions (C96 AEC-Q200 soft termination, 10 mm from the edge)	Crack or dielectric short, hard	48V/12V_BDC shorted	BDC-MLCC-B		1.80	25%	0.450	n/a			·	·	·	·	**Direct**	**SM-70**	90%	·	0.045	·	0.405			EPB-201, EPB-423	The EPB-423 overcurrent trip on Q11 is meant to keep the service brake powered (SG-02); for SG-07 U1 remains the credited mechanism.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC JUDGMENT OQ-028
F07-054	C96, C97	EPB bulk with actions (C96 AEC-Q200 soft termination, 10 mm from the edge)	Crack short, resistive	Up to about 1 kW at C96 or C97 below the U1 band	BDC-MLCC-B		1.80	25%	0.450	n/a			·	·	·	·	**Direct**	**SM-71**	60%	·	**0.180**	·	0.270			EPB-201, PCB-202	EPB-423's trip as written is set above the EPB stall current and does not see this. An idle-current trip on the Q11 sense (branch current above about 0.5 A with U7 idle) would; it is proposed in the notes, not credited.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT; DC PROVISIONAL OQ-044
F07-055	C96, C97	EPB bulk with actions (C96 AEC-Q200 soft termination, 10 mm from the edge)	Open or capacitance loss	No SG-07 effect	BDC-MLCC-B		1.80	50%	0.900	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-018; share JUDGMENT (class split)

Failure modes										VerB as built							With DFMEA actions							Traceability				
ID	Element	Part	Failure mode	Effect on the goal if not controlled	FIT key	Qty	λ part × qty (FIT)	Mode share	λ mode (FIT)	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Class	Mechanism	DC	λ SPF	λ RF	λ MPF latent	λ MPF detected	Partner rows (dual-point)	Partner λ (FIT)	DFMEA rows	Remarks	ASSUMED values
F07-056	U7	DRV8263-Q1	VM-to-GND internal short, hard (half of F03-009)	48V/12V_BDC shorted inside U7	U7		20.00	3%	0.500	**Direct**	SM-70	90%	·	0.050	·	0.450	**Direct**	SM-70	90%	·	0.050	·	0.450			EPB-201		λ GATED OQ-007; share JUDGMENT; DC JUDGMENT OQ-028
F07-057	U7	DRV8263-Q1	VM-to-GND internal short, resistive	U7 package heats on the live 48V/12V_BDC below the U1 band	U7		20.00	3%	0.500	**Direct**			**0.500**	·	·	·	**Direct**	**SM-71**	60%	·	**0.200**	·	0.300			EPB-201	U7 thermal shutdown protects the output stage, not a VM-to-GND leak.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-044
F07-058	U7	DRV8263-Q1	Other U7 faults (output stage, logic, OCP and thermal shutdown lost)	No SG-07 effect	U7		20.00	95%	19.000	n/a			·	·	·	·	n/a			·	·	·	·			EPB-203, EPB-214, EPB-221	EPB outputs carry current only for about a second per actuation (self-locking spindle), so a resistive output fault cannot accumulate heat; a hard one trips U7 OCP or, beyond it, U1.	λ GATED OQ-007; share JUDGMENT
F07-060	U2	LM68645-Q1	VIN-to-PGND internal short, hard	48V/12V_P shorted inside U2	U2		20.00	3%	0.500	**Direct**	SM-70	90%	·	0.050	·	0.450	**Direct**	SM-70	90%	·	0.050	·	0.450			BCK-103		λ GATED OQ-007; share JUDGMENT; DC JUDGMENT OQ-028
F07-061	U2	LM68645-Q1	VIN-to-PGND internal short, resistive	U2 package heats below the U1 band	U2		20.00	3%	0.500	**Direct**			**0.500**	·	·	·	**Direct**	**SM-71**	60%	·	**0.200**	·	0.300			BCK-103	U2 thermal shutdown acts on its switching, not on a VIN-to-PGND leak.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-044
F07-062	U2	LM68645-Q1	High-side FET short: 12 V rail pulled toward 48V/12V_P	25 V capacitors C27, C31-C33 and U3 VBAT at 48-60 V break down: a resistive 48 V short on the 12 V rail	U2		20.00	10%	2.000	**Direct**	SM-09	90%	·	**0.200**	·	1.800	**Direct**	SM-09	90%	·	**0.200**	·	1.800			BCK-101, PMC-102	SM-09 removes 48V/12V_P in about 2 ms (SDAA375), before the broken-down parts can heat. Same share as F03-120 and F01-100.	λ GATED OQ-007; share JUDGMENT; DC PROVISIONAL OQ-014
F07-063	U2	LM68645-Q1	Cycle-by-cycle current limit or hiccup lost	A hard 12 V short is no longer limited (latent)	U2		20.00	3%	0.600	Latent			·	·	0.600	·	Latent			·	·	0.600	·	F07-070, F07-073	4.90	BCK-102, BCK-104	No test of the U2 current limit; full λ latent. Share is sev10's (TI FMEDA on request, OQ-007).	λ GATED OQ-007; share JUDGMENT
F07-064	U2	LM68645-Q1	Output low or lost, other regulation faults	No SG-07 effect (12 V lost: corner resets)	U2		20.00	82%	16.400	n/a			·	·	·	·	n/a			·	·	·	·			BCK-102, PMC-117	No thermal path.	λ GATED OQ-007; share JUDGMENT
F07-065	R33, R35	100 kOhm, 7.15 kOhm 0402 (U2 feedback)	R33 open or R35 short: U2 drives 12 V toward the input	As F07-062: 25 V parts on the 12 V rail break down under 48-60 V	RES-0402	2	0.60	35%	0.210	**Direct**	SM-09	90%	·	0.021	·	0.189	**Direct**	SM-09	90%	·	0.021	·	0.189			BCK-201, BCK-202	Share as F01-102.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC PROVISIONAL OQ-014
F07-066	R33, R35	100 kOhm, 7.15 kOhm 0402 (U2 feedback)	R33 short, R35 open, drift within tolerance	No SG-07 effect (12 V low)	RES-0402	2	0.60	65%	0.390	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-070	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors as built (C25 GRM 1210; C27, C31-C33 GRM 0805 X5R 25 V, 85 C)	Short, hard (below the U2 hiccup entry)	12 V collapses; U2 limits and hiccups	CAP-12V		13.30	25%	3.325	**Direct**	SM-72	90%	·	**0.333**	·	2.993	n/a			·	·	·	·			BCK-104, BCK-403	Replaced in part by the actions (row F07-073).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC GATED OQ-007
F07-071	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors as built (C25 GRM 1210; C27, C31-C33 GRM 0805 X5R 25 V, 85 C)	Crack or wear-out short, resistive (about 1-15 Ohm)	U2 holds 12 V in regulation and feeds 10-70 W into the part: charring; C25 sits 0.58 mm from C22 on 48V/12V_P	CAP-12V		13.30	25%	3.325	**Direct**			**3.325**	·	·	·	n/a			·	·	·	·			BCK-403, BCK-104, BCK-409	BCK-403: 'no monitor sees it until the board chars'. 0.9 A at 54 V is below any IMON resolution.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-072	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors as built (C25 GRM 1210; C27, C31-C33 GRM 0805 X5R 25 V, 85 C)	Open or capacitance loss	No SG-07 effect	CAP-12V		13.30	50%	6.650	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-073	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors with actions (C25 soft termination; C27, C31-C33 AEC-Q200 X7R 50 V, 125 C)	Short, hard	12 V collapses; U2 limits and hiccups	CAP-12V-B		6.30	25%	1.575	n/a			·	·	·	·	**Direct**	**SM-72**	90%	·	**0.158**	·	1.418			BCK-104, BCK-403, BCK-409		λ NO-CLIENT-DATA OQ-010; share JUDGMENT; DC GATED OQ-007
F07-074	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors with actions (C25 soft termination; C27, C31-C33 AEC-Q200 X7R 50 V, 125 C)	Short, resistive	10-70 W in one part below any limit	CAP-12V-B		6.30	25%	1.575	n/a			·	·	·	·	**Direct**			**1.575**	·	·	·			BCK-403	The BCK-403 detect action adds a 12 V current limit only if the fault injection fails; not credited.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-075	C25, C26, C27, C31-C36, C89, C62	12 V rail capacitors with actions (C25 soft termination; C27, C31-C33 AEC-Q200 X7R 50 V, 125 C)	Open or capacitance loss	No SG-07 effect	CAP-12V-B		6.30	50%	3.150	n/a			·	·	·	·	n/a			·	·	·	·				No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split)
F07-080	Q4, Q5, Q7-Q10	SQJA90EP	Drain-source short	Shoot-through at the next switching; the leg ends as a hard 48V/12V_P short	FET-80V	6	60.00	40%	24.000	**Direct**	SM-70	90%	·	**2.400**	·	21.600	**Direct**	SM-70	90%	·	**2.400**	·	21.600			BLD-201	The U5 VDS monitor stops the first shoot-through if configured (thresholds unpublished, OQ-007) and is not credited; U1 is the independent backstop (BLD-201). A die-melt short is hard.	λ JUDGMENT OQ-010; share JUDGMENT (class split); DC JUDGMENT OQ-028
F07-081	Q4, Q5, Q7-Q10	SQJA90EP	Drain-source open, gate-source short, on-resistance increase	No SG-07 effect (phase lost or lossy)	FET-80V	6	60.00	60%	36.000	n/a			·	·	·	·	n/a			·	·	·	·			BLD-202, BLD-210, PCB-403	On-resistance increase heats the FET by the load current only; it ends open or shorted (F07-080) before the laminate reaches Td (JUDGMENT).	λ JUDGMENT OQ-010; share JUDGMENT (class split)
F07-082	J7, J8, J9	Motor phase wire pads	Joint degrades to high resistance and heats (half of the 70 % open mode)	Pad and wire overheat at phase current while the motor holds or builds force	PAD	3	1.50	35%	0.525	**Direct**			**0.525**	·	·	·	**Direct**			**0.525**	·	·	·			PCB-502	A service-brake motor may hold current for long periods (unlike the self-locking EPB). No path-resistance check exists (PCB-502 'requires SW' only).	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-083	J7, J8, J9	Motor phase wire pads	Clean open (crack, lift)	No SG-07 effect (phase lost)	PAD	3	1.50	35%	0.525	n/a			·	·	·	·	n/a			·	·	·	·			BLD-213	No thermal path.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT
F07-084	J7, J8, J9	Motor phase wire pads	Short to an adjacent phase pad or to the harness	Two legs or a leg and GND shorted through the bridge	PAD	3	1.50	30%	0.450	**Direct**	SM-70	90%	·	0.045	·	0.405	**Direct**	SM-70	90%	·	0.045	·	0.405			BLD-212, PCB-102	A pad bridge or strand is metallic: hard. U5 VDS first (not credited), U1 as backstop.	λ NO-CLIENT-DATA OQ-010; share JUDGMENT (class split); DC JUDGMENT OQ-028
F07-090	!PCB1 48V/12V_P, 48V/12V_BDC	CAF path to GND, 0.41-0.50 mm, laminate unspecified	CAF filament grows to a resistive path	Up to about 1 kW in the laminate below the U1 band (PCB-303)	CAF-48V	2	2.00	100%	2.000	**Direct**			**2.000**	·	·	·	n/a			·	·	·	·			PCB-303, PCB-306	Replaced by the CAF-resistant laminate and wider inner spacing of the actions (row F07-091).	λ JUDGMENT OQ-016; share JUDGMENT (class split)
F07-091	!PCB1 48V/12V_P, 48V/12V_BDC	CAF path to GND, CAF-resistant laminate, >= 0.5 mm	CAF filament grows to a resistive path	Heat in the laminate below the U1 band	CAF-48V-R	2	0.40	100%	0.400	n/a			·	·	·	·	**Direct**	**SM-71**	60%	·	**0.160**	·	0.240			PCB-303	Both nets are downstream of R7 and live at idle, so the idle IMON check applies.	λ JUDGMENT OQ-016; share JUDGMENT (class split); DC PROVISIONAL OQ-044
F07-092	!PCB1 input nets and phases	CAF path to GND: 48V/12V_IN, 48V/12V_IN_FILTERED, NetC7_2, NetQ2_5 (0.40-0.53 mm); SHA, SHB, SHC (0.40-0.42 mm)	CAF filament grows to a resistive path	Input side: heat ahead of R7 with only the vehicle fuse behind it; phases: heat while the bridge drives	CAF-48V	7	7.00	100%	7.000	**Direct**			**7.000**	·	·	·	n/a			·	·	·	·			PCB-302, PCB-303	The input nets stay biased while the vehicle is parked (about 131,000 h calendar life against 8,000 operating hours; OQ-055). Replaced by row F07-093.	λ JUDGMENT OQ-016; share JUDGMENT (class split)
F07-093	!PCB1 input nets and phases	CAF path to GND, CAF-resistant laminate, >= 0.5 mm	CAF filament grows to a resistive path	As F07-092	CAF-48V-R	7	1.40	100%	1.400	n/a			·	·	·	·	**Direct**			**1.400**	·	·	·			PCB-302, PCB-303	Ahead of R7 nothing on the board sees it; on the phases IMON is masked by the drive current and the nets are unbiased at idle. Not covered by SM-71.	λ JUDGMENT OQ-016; share JUDGMENT (class split)
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
													·	·	·	·				·	·	·	·					
Σ			**Totals. Σλ counted per scenario excludes n/a rows; the metrics above use these sums.**							**71.66 λ**			**23.950**	**4.504**	**5.522**	**37.682**	**57.66 λ**			**7.550**	**6.309**	**5.592**	**38.207**					

SPFM = 1 − Σ(λ SPF + λ RF) / Σλ counted. LFM = 1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF). PMHF = Σλ SPF + Σλ RF + Σ(λ MPF,latent × partner λ) × lifetime / 10⁹. ISO 26262-5:2018 clauses 8 and 9, Annex C. λ MPF,detected is shown for completeness; its exposure over the test interval is neglected (Basis tab).

ID	Kind	Mechanism	Implemented by	ISO 26262-5 Annex D basis	DC as built	DC with actions	Basis for the DC	DFMEA rows	Rows using it	Reason code	Closes with
SM-01	Prevents violation	MCU lockstep cores, ECC and error-signal module; the PMIC resets the MCU on an error	HW in U14 (TI)	Processing units: hardware redundancy, dual-core lockstep (High)	99% ASSUMED	99% ASSUMED	TI claims High coverage for the lockstep MCU; the value needs TI's safety manual and FMEDA	EPB-101	4	GATED	OQ-007
SM-02	Prevents violation	PMIC watchdog and error monitor reset the MCU; its pins float and U7 turns off (DRVOFF high)	HW on VerB (U7 internal pull-up); with actions: external DRVOFF pull-up and SAFE_OUT1 to U7 nSLEEP	Watchdog with separate time base and time window (Medium); with an independent de-energising path (High)	90% ASSUMED	90% ASSUMED	A watchdog with its own time base is Medium at most (Annex D); the SAFE_OUT1 path the actions add improves the reaction, not the detection. As built the stop relies on the U7-internal DRVOFF pull-up	EPB-101, EPB-121, EPB-408	2	PROVISIONAL	OQ-002
SM-03	Prevents violation	EPB current plausibility (IPROPI current with no command stops the bridge)	SW; reaction through DRVOFF (same die as the fault) as built, through the Q11 cut-off with actions	Monitoring of outputs, plausibility check (Low as built, reaction in the same die; Medium with an independent switch)	60% ASSUMED	**90% ASSUMED**	As built the only reaction acts inside U7, the device that failed; with R58 not fitted the Q11 cut-off stops the bridge independently. Opening Q11 ends the apply but does not release the force built so far; the credit assumes the stop comes before that force is hazardous (EPB-409, OQ-047) For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052).	EPB-103, EPB-112	3	PROVISIONAL	OQ-032
SM-04	Prevents violation	Independent EPB terminal-voltage readback (OUTA/OUTB) with Q11 cut-off reaction	Not on VerB; with actions: dividers to spare MCU ADC inputs, Q11 drive restored	Monitoring of outputs with independent read-back and an independent switch-off path (Medium)	0% ASSUMED	**90% ASSUMED**	As built nothing observes the motor terminals independently of U7 and the cut-off cannot open (R58 fitted); the IPROPI mirror is blind to a shorted high-side FET (EPB-314). The Q11 reaction ends the apply without releasing it; the credit assumes the stop comes before the force is hazardous (EPB-409, OQ-047) For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052).	EPB-211, EPB-314, EPB-401	2	PROVISIONAL	OQ-029
SM-05	Prevents violation	SPI integrity for U7 (REG_LOCK, SPI_IN lock, cyclic readback of COMMAND, SPI_IN and CONFIG, status byte check)	SW	Information redundancy, read-back of configuration (Medium; the frame has no CRC)	90% ASSUMED	90% ASSUMED	A correctly framed wrong write is caught only by readback; no CRC on the DRV8263 frame	EPB-501, EPB-502, EPB-512	4	PROVISIONAL	OQ-032
SM-06	Prevents violation	Direction plausibility of EPB motion (a release that ends in a rising current to stall is an apply; an apply that ends at the release end stop is a release)	SW; from the unsigned current profile as built, from the terminal voltages with actions	Plausibility check of outputs (Low as built; Medium with terminal readback)	60% ASSUMED	**90% ASSUMED**	The IPROPI current has no sign, so as built the direction is inferred from the profile only For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052).	EPB-104, EPB-113	4	PROVISIONAL	OQ-032
SM-07	Prevents violation	Standstill confirmed by an independent source (other rear wheel or vehicle speed over CAN); loss of pulses is invalid, never standstill	SW	Plausibility check with an independent redundant sensor (High)	99% ASSUMED	99% ASSUMED	The independent source is on another ECU; the rule and the standstill threshold (OQ-035) must be in the technical safety concept	WSS-315, WSS-118, EPB-519	4	PROVISIONAL	OQ-038
SM-08	Prevents violation	PMIC rail monitoring (EXT_VMON1 on the 1.25 V core; LDO1, LDO2 and LDO3 over- and undervoltage) resets U14; the drivers turn off	HW in U3 (TI), thresholds and reaction in NVM	Power supply: voltage monitoring of the output with a reaction (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	TI claims monitoring of every rail, but the thresholds, deglitch and reaction time sit in the NVM of the fitted variant and the LDO1 monitor shares the die with the regulator; PMC-304 asks whether the core monitor acts before the U14 absolute maximum	PMC-203, PMC-206, PMC-303, PMC-304, WSS-111	13	GATED	OQ-002
SM-09	Prevents violation	12 V overvoltage cut-off (U14 CMPSS window on VMON drives nSTB_CAN low; both transceivers drop INH; U1 removes 48V/12V_P)	HW path configured by firmware at start-up (CMPSS, output crossbar), acting without the CPU	Power supply: voltage monitoring of the input with a switch-off (Medium)	90% ASSUMED	90% ASSUMED	TI measured about 2 ms from 13.2 V to 12 V off (SDAA375); the path runs through QM transceivers and firmware configuration (OQ-014)	PMC-102, BCK-101, BCK-201, BCK-202	6	PROVISIONAL	OQ-014
SM-10	Prevents violation	BLDC current and force plausibility against the request (phase current with no command, current against commanded duty) asserts DRVOFF and nSLEEP	SW in U14; reaction on U14.87/U14.86, pins other than the PWM outputs	Monitoring of outputs, plausibility check (Medium claimable)	60% ASSUMED	**80% ASSUMED**	Detects PWM port faults the lockstep cannot see. Reaction STOP only (U5 gates off; release by A-08, PMC-419). As built no threshold, idle-case check or force reference is specified (force is estimated from current and angle, no force sensor): Low. With BLD-108's per-phase check at idle and its HIL test: 0.80, below the Medium ceiling because a fault that makes current look plausible (wrong but commanded pattern) escapes.	BLD-101, BLD-108	1	PROVISIONAL	OQ-032
SM-11	Prevents violation	Motor phase isolation driven independently of U5 (U14 GPIO and PMIC SAFE_OUT1), opened on a VDS/Rsense fault or on phase current with no command	Not on VerB; with actions: back-to-back FETs in two phases (BLD-201) with a drive that does not use U5 outputs (BLD-118, BLD-227)	Monitoring of outputs with an independent switch-off path (Medium)	0% ASSUMED	**90% ASSUMED**	As built nothing removes motor current independently of U5, and nothing frees a motor braked by a shorted phase. With the actions two independent detections (U5 VDS monitor and U14 phase current) feed a reaction outside U5; that argues for the Medium ceiling. Reaction frees the motor, then release is by A-08 (STOP, PMC-419). Driving the isolation from the DRV3263A CUTOFF2 channel, as BLD-201 suggests, would not qualify for U5 die faults.	BLD-118, BLD-201, BLD-227	3	PROVISIONAL	OQ-023

ID	Kind	Mechanism	Implemented by	ISO 26262-5 Annex D basis	DC as built	DC with actions	Basis for the DC	DFMEA rows	Rows using it	Reason code	Closes with
SM-12	Prevents violation	Phase-current plausibility (three-shunt sum, voltage/speed model, zero-current offset at standstill, range check, CSA gain readback) stops the drive; the corner is reported unavailable in the next status frame	SW in U14; with actions also one phase converted on a second ADC (BLD-315)	Plausibility check of redundant measurements (Medium claimable)	60% ASSUMED	**80% ASSUMED**	Single-phase errors break the sum; rail-level readings fail the range check. A common gain error on all three phases passes both and is left to force-versus-position plausibility (BLD-315): Low as built. The second-ADC compare of BLD-315 lifts it, but not to the Medium ceiling while the force reference is itself estimated. Reaction STOP (PMC-419).	BLD-301, BLD-312, BLD-315, BLD-320, SUP-322	15	PROVISIONAL	OQ-038
SM-13	Prevents violation	U5 SPI integrity (register lock where available, cyclic readback of all configuration registers within 100 ms, all-ones/all-zero frame rejection); the corner is reported unavailable in the next status frame	SW	Information redundancy, read-back of configuration (Medium)	80% ASSUMED	80% ASSUMED	Whether the DRV3263 frame carries a CRC is in the NDA safety manual (OQ-007); readback alone catches a persistent wrong configuration but not a transient one between reads, so below the Medium ceiling. Reaction DRVOFF/nSLEEP, which still works for this mode (STOP, PMC-419).	BLD-114, BLD-115, BLD-313	3	PROVISIONAL	OQ-032
SM-14	Prevents violation	Angle plausibility (U12/U13 channel compare, sin^2+cos^2 window, 10-90 % range, quadrant consistency, motion check) stops the drive and reports	SW in U14; with actions also 100 kOhm pull-downs and 10 nF filters (ANG-101, ANG-112)	Comparison of redundant sensors (High claimable)	90% ASSUMED	**97% ASSUMED**	Credited for single-channel faults only; faults common to both channels are separate rows with their own mechanism (SM-15) or none. As built a sensor in its safe state holds a plausible value on 0.1 uF and is seen only when the rotor moves, and no threshold or debounce is derived (ANG-309): 0.90. With the pull-downs and a derived threshold 0.97, below the High ceiling because slow in-range drift below the threshold is not seen. Reaction STOP (PMC-419).	ANG-101, ANG-309	10	PROVISIONAL	OQ-038
SM-15	Prevents violation	Independent analog reference check (a known voltage converted each cycle) with the two angle channels on different ADC modules	Not possible on VerB (MCU-302); with actions: reference on a separate module, ch1 on ADC A/B, ch2 on ADC C/D	Test of analog input with a reference (Medium)	0% ASSUMED	**80% ASSUMED**	Covers LDO1/LDO3 drift inside the PMIC window and ADC faults common to both angle channels. Below the Medium ceiling: a ratiometric error that scales the reference and the sensors together (LDO1 feeds both) is only partly visible. Reaction STOP (PMC-419).	PMC-201, MCU-302, ANG-306, ANG-113	4	PROVISIONAL	OQ-038
SM-16	Prevents violation	End-to-end protection of the clamp-force request (CRC, alive counter, per-corner data ID, timeout) with release to zero force on failure	SW (AUTOSAR E2E or equivalent)	Communication bus: information redundancy with frame counter and timeout monitoring (High claimable)	90% ASSUMED	90% ASSUMED	The profile is not specified, and a request meant for another corner is rejected only if the ECU knows its own position (OQ-040): Medium credited. Reaction REL: U14 and U5 are healthy for these faults, so U14 commands the release and reports the corner unavailable.	CAN-102, CAN-131, CAN-209, MCU-508	2	PROVISIONAL	OQ-040
SM-20	Prevents violation	Cross-wheel speed plausibility in the brake controller (deviation from the vehicle reference speed above max(2 km/h, 5 %) for 20 ms, or wheel acceleration beyond the physical limit, marks the wheel invalid)	SW in the brake controller (another ECU); assumption of use for this SEooC	Sensor rationality check against redundant sensors (Medium)	80% ASSUMED	80% ASSUMED	Detects gross errors only. It misses deviations below the threshold (ASSUMED; a small offset from U6, the capture path or the clock passes). It also misses low readings during an ABS or ESC intervention, where they look like a locking wheel until the vehicle-reference and wheel-acceleration checks reject them. Timing: speed update 10 ms + CAN cycle 10 ms + 20 ms confirmation = 40 ms, within the 50 ms FTTI above about 10 km/h (48 teeth, 2.0 m, OQ-035). Below that speed the pulse period stretches the detection, but ABS and ESC are assumed inactive there.	WSS-119, WSS-204, WSS-213, WSS-215, WSS-216	9	PROVISIONAL	OQ-049
SM-21	Prevents violation	MCU clock monitoring: missing-clock detection (limp to INTOSC, CLOCKFAIL) and the DCC comparing X1/PLLRAWCLK with INTOSC continuously; on an error the wheel speed is sent invalid; the corner is reported unavailable in the next status frame	HW in U14, configured by firmware (DCC off after reset)	Clock: monitoring with an independent time base (Medium)	90% ASSUMED	90% ASSUMED	The MCD detects every absent clock in hardware, and the DCC runs continuously. Errors inside the INTOSC tolerance (about 3 %) are not claimed; they are separate rows (F05-071, F05-072), so the Medium value is kept on the rows it covers. The reaction marks the speed invalid in the next 10 ms frame, within the FTTI. The configuration and its coverage come from the F29P32x safety manual (MCU-204).	MCU-201, MCU-202, MCU-203, MCU-204	6	GATED	OQ-007
SM-22	Prevents violation	U6 configuration readback and reset detection over SPI-D every 10 ms (status/reset flag, configuration registers against the written values, fixed-field frame check); a mismatch re-initialises U6 and marks the speed invalid until readback passes	SW in U14	Information redundancy, read-back of configuration (Medium)	80% ASSUMED	80% ASSUMED	The WSS001 register map, reset flag and frame integrity are unknown, and an internal fault that changes the decoder without changing the register image is not seen, so the value is below the Medium ceiling. Reaction within 20 ms plus one CAN cycle.	WSS-121, WSS-122, WSS-307, WSS-311, WSS-312, WSS-313, EPB-519	2	UNRELEASED	OQ-008
SM-23	Prevents violation	Loss-of-pulse check: no WSSO edge for two expected periods (from the vehicle reference) while the reference is above 5 km/h marks the wheel invalid, never zero or standstill	SW in the brake controller (assumption of use); may be duplicated in U14 using the vehicle speed over CAN	Sensor rationality check against redundant sensors (Medium)	90% ASSUMED	90% ASSUMED	A zero against a moving reference is unambiguous except during an ABS intervention, where it looks like a locked wheel until the lock-time limit, which may exceed the FTTI. ABS intervention is a small fraction of operating time, so the Medium value is argued. Timing: two periods at 10 km/h = 30 ms + CAN 10 ms. Differs from SM-07 (0.99), which rates the standstill decision for SG-03 with no braking dynamics.	WSS-118, WSS-202, WSS-203, WSS-206, WSS-207, WSS-209, WSS-301, WSS-302	14	PROVISIONAL	OQ-049
SM-24	Prevents violation	End-to-end protection of the wheel-speed signal and its validity flag (CRC, alive counter, timeout of 3 cycles) checked by the brake controller; failure or timeout marks the wheel invalid	SW in U14 (sender) and the brake controller (receiver)	Communication bus: information redundancy with frame counter and timeout monitoring (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	Same basis as LM-08. The profile, cycle (10 ms assumed) and timeout (30 ms assumed) are not specified, so the Medium value is credited. A 30 ms timeout is inside the 50 ms FTTI.	MCU-508, CAN-112, CAN-214, PMC-207	5	PROVISIONAL	OQ-040

ID	Kind	Mechanism	Implemented by	ISO 26262-5 Annex D basis	DC as built	DC with actions	Basis for the DC	DFMEA rows	Rows using it	Reason code	Closes with
SM-30	Prevents violation	Corner-status timeout in the brake controller: this corner's status frame (CRC, alive counter, 10 ms cycle) missing, frozen or corrupt beyond the timeout marks the corner unavailable; the other corners and regeneration compensate and the driver is warned	SW in the brake controller (another ECU), assumption of use for this SEooC; U14 sends the status frame on both CAN channels	Communication bus: information redundancy with frame counter and timeout monitoring (High claimable)	90% ASSUMED	90% ASSUMED	The only way the brake controller learns of a corner that loses U14 or both CAN channels (rail, reset or supply faults, PMC-118). A node that has gone silent, or a transmitter that repeats a frozen frame, cannot pass a timeout with an alive counter, so High is argued once the check exists. As built nothing specifies it: no status frame profile, timeout value or reaction (OQ-022, OQ-040), and a U14 that reboots faster than the timeout would come back reporting "available" (PMC-419): Medium, as SM-24. With the actions PMC-118 makes it a vehicle safety requirement proved by HIL fault injection (VCC_6V0 to GND during braking, flagged within 200 ms), and PMC-419's reset-cause rule keeps the corner "unavailable" after an unplanned reset until its start-up tests pass. Timeout monitoring alone is credited at Medium in both scenarios, consistent with SM-24; High would follow from the specified profile and the HIL proof. Timing: 10 ms cycle, 3-frame timeout (30-50 ms) plus redistribution, within the 200 ms provisional FTTI (OQ-021).	PMC-118, PMC-419, CAN-302, CAN-303	16	PROVISIONAL	OQ-022
SM-31	Prevents violation	Drive-response monitor in U14: commanded current or duty with no or too little phase current (per phase and total), no rotor motion under breakaway current, or U5 nFAULT/SPI fault status; reaction: drive off and corner reported unavailable or limited in the next status frame	SW in U14 using the phase-current ADC channels, the angle and nFLT_DRV3263 (U14.85)	Monitoring of outputs, plausibility check of the actuator response (Medium claimable)	60% ASSUMED	**90% ASSUMED**	Detects a drive that no longer follows its command whatever the cause (U5 outputs off, lost gate supply, open FET, phase or shunt, PWM or disable pin stuck), which is silent otherwise because the corner keeps reporting "available". As built the DFMEA only asks for it (BLD-104, BLD-110, BLD-202): no threshold, time or reaction: Low. With BLD-104's 50 ms threshold, BLD-110/BLD-202's per-phase check and their fault-injection tests, the Medium ceiling is argued: a lost or open phase is a gross, unambiguous discrepancy between command and current. Not claimed: a slow build-up that stays within current limits (FE-06), which needs the response budget of BLD-225 (OQ-021). Reaction RPT: U14 is healthy for every mode it is credited on.	BLD-104, BLD-110, BLD-202, BLD-305, BLD-503, BLD-225	14	PROVISIONAL	OQ-032
SM-32	Prevents violation	MCU lockstep, ECC and ESM (SM-01) reset U14; the corner is then silent and reported by the status timeout (SM-30)	HW in U14 (TI), then SW in the brake controller	Dual-core lockstep (High) in series with timeout monitoring (High claimable)	89% ASSUMED	**89% ASSUMED**	Detection alone does not reach the SG-02 safe state: the reset silences the corner and the brake controller learns of it only by SM-30. Coverage taken as the product of the two, SM-01 × SM-30: 0.99 × 0.90 as built, 0.99 × 0.99 with the actions.	MCU-503, PMC-118, PMC-419	1	GATED	OQ-007
SM-33	Prevents violation	PMIC watchdog and error monitor (SM-02) reset U14; the corner is then silent and reported by the status timeout (SM-30)	HW in U3 (TI), then SW in the brake controller	Watchdog with separate time base (Medium) in series with timeout monitoring	81% ASSUMED	81% ASSUMED	Product SM-02 × SM-30: 0.90 × 0.90 in both scenarios (SM-30 is Medium in both). A U14 that stops its status frames is seen by the timeout even if the watchdog misses it, so the product is conservative.	MCU-507, PMC-402, PMC-118	1	PROVISIONAL	OQ-002
SM-34	Prevents violation	PMIC rail monitoring (SM-08, all LDOs, BB_OUT and EXT_VMON1) resets U14; the corner is then silent and reported by the status timeout (SM-30)	HW in U3 (TI, thresholds and reaction in NVM), then SW in the brake controller	Voltage monitoring with a reaction (Medium credited) in series with timeout monitoring	81% ASSUMED	81% ASSUMED	Product SM-08 × SM-30: 0.90 × 0.90 in both scenarios (SM-30 is Medium in both). The LDO1 undervoltage threshold must sit above 2.65 V or both angle channels freeze before the reset (ANG-305, OQ-002).	PMC-203, PMC-206, PMC-303, ANG-305, PMC-118	3	GATED	OQ-002
SM-40	Prevents violation	Hold hand-over on unintended EPB motion at standstill: current on Isense_EPB (as built) or OUTA/OUTB terminal voltage (with actions) with no command reports 'hold lost at this corner' over CAN; the other rear corner re-clamps, the driver is warned and the park lock is requested	SW in U14 (detection, report); the re-clamp by the other rear corner is an assumption of use (vehicle level). With actions the Q11 cut-off and SAFE_OUT1 also stop the motion	Monitoring of outputs, plausibility check (Low as built; Medium with independent read-back and a reaction outside the failed part)	60% ASSUMED	**90% ASSUMED**	Credited where the EPB drive path itself cannot be used for the reaction (U14 EPB pins stuck): the report does not need the stuck pins. As built there is no threshold or debounce, the IPROPI mirror is blind to current that does not pass a gate-driven high-side FET (EPB-314), nothing stops the release, so this corner loses all its force and the hold rests on the other corner alone: Low. With the actions the terminal readback gives a second observation and Q11/SAFE_OUT1 stop the release, so the spindle keeps what is left: the Medium ceiling is argued on two independent observations and a reaction outside the failed part. Not High: the other corner's re-clamp and its timing within the 1 s FTTI are not specified (new question on single-corner hold).	EPB-101, EPB-211, EPB-314, EPB-408	1	PROVISIONAL	OQ-032

ID	Kind	Mechanism	Implemented by	ISO 26262-5 Annex D basis	DC as built	DC with actions	Basis for the DC	DFMEA rows	Rows using it	Reason code	Closes with
SM-41	Prevents violation	Apply-completion check on every park and auto-hold apply (inrush within a set time, stall reached within the expected window, U7 STATUS/FAULT and VMUV read, SPI health); a failed apply is repeated once, then the EPB is reported unavailable, the driver is warned, the other rear corner holds and the park lock is requested	SW in U14; the vehicle reaction (warning, other corner, park lock) is an assumption of use	Monitoring of outputs, plausibility of the effect against the command (Medium)	90% ASSUMED	90% ASSUMED	Covers faults that leave the EPB unable to drive (U7 outputs off, Q11 or its drive open, pads open, U7 asleep or held off). A held EPB keeps its force when these faults occur (self-locking, OQ-023); they matter at the next apply, where the absence of current or of a stall is unambiguous. The check runs on every apply and reports before the driver leaves the vehicle, and its reaction does not use the failed part, so the Medium ceiling is argued. Not High: the hold after the report relies on the other corner and the park lock (vehicle level), and a fault that lets current flow but weakens the force is left to SM-42. Same value in both scenarios: the check uses the as-built current sense.	EPB-106, EPB-108, EPB-111, EPB-207, EPB-212, EPB-414, EPB-415, EPB-416, EPB-510	18	PROVISIONAL	OQ-032
SM-42	Prevents violation	Holding-force plausibility of each apply: rest-offset check of Isense_EPB before the apply, stall accepted only after a minimum run time or ripple travel, stall current compared with the value expected at the measured supply; a failed check re-applies once, then reports as SM-41	SW in U14	Plausibility check of a sensor against a model (Low)	60% ASSUMED	60% ASSUMED	Catches a reading stuck high or offset (rest check) and an apply that stalls too early (run time), but not a gain error inside the plausibility window: there is no second measurement of EPB current or force (EPB-309, EPB-318). The actions add no second measurement, so Low in both scenarios. A current reading that is too high is safe-side for SG-03 (an early stop) and the hazard for SG-04 (an early false stall).	EPB-303, EPB-304, EPB-306, EPB-309, EPB-318, EPB-321	5	PROVISIONAL	OQ-043
SM-43	Prevents violation	End-to-end protection of the EPB release and drive-away request (CRC over the payload read from message RAM, alive counter, data ID, timeout) with 'keep the hold' as the reaction to any failure	SW in U14 (AUTOSAR E2E or equivalent)	Communication bus: information redundancy with frame counter and timeout monitoring (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	Same basis as SM-16 and LM-08: the profile and data ID are not specified, so Medium is credited. The reaction differs from SM-16 (release to zero force): for a parking or standstill-hold request a failed check keeps the hold, which needs no working actuator.	CAN-101, CAN-209, MCU-508	1	PROVISIONAL	OQ-040
SM-70	Prevents violation	U1 short-circuit comparator (26.9-34 A, 3.5-5.5 us) and circuit breaker (18-27 A, about 1 ms) open Q1 and latch off (R21 across C_TMR); the corner is unpowered and reported by CAN timeout at the brake controller	HW in U1 (TI), thresholds set by R7, R11, R20, R_ISCP and the TMR network	Power supply: current control of the output (48V/12V_P) with switch-off (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	Credited only on the rows defined as hard (above the breaker band) downstream of R7, so the resistive faults it cannot see are not in its coverage. Kept below the High ceiling because a crack or bridge that sputters (intermittent contact, carbon path forming and burning off) can drop below 18 A before the 1 ms timer ends and restart it, and the thresholds carry the R7, R11 and IMON-free tolerance of the set network (SUP-314); nothing tests the comparators (their loss is latent, F07-020, F07-021, F07-026). Acts in microseconds to a millisecond, far inside any time to ignition. The 1.4-1.6 J the bulk dumps into the fault first is not a sustained source.	EPB-201, BLD-401, SUP-417, PCB-202, SUP-314	9	JUDGMENT	OQ-028
SM-71	Prevents violation	Supply-current check on U1 IMON (U14.35, 0.135 V/A): with both bridges idle, IMON above the known quiescent draw plus about 3 A pulls INH_CAN low (U1 off), latches the corner off and reports it; while driving, IMON against the phase-shunt sum and the EPB current	Not on VerB; with actions: SW in U14 (PCB-202 SW safety requirement, SUP-314 detect action), reaction through INH and U1 EN	Power supply: current monitoring by plausibility, reaction by switch-off (Low)	0% ASSUMED	**60% ASSUMED**	IMON resolves about 3 A (offset +/-2.1 mV = +/-2.1 A at 1 mOhm, gain +/-12.5 %), about 160 W at 54 V, so resistive faults of 2-3 A and the low-power start of a crack or CAF path are missed (PCB-202). The Low ceiling is argued because the covered high-power end is the part that ignites fastest, and a carbonising path tends to fall in resistance into the covered band before it ignites. It runs only downstream of R7 and only with the bridges idle for the idle check; the drive-time balance is not credited. Check period and debounce must sit inside the time to ignition at about 1 kW, which is unknown (OQ-044). Reaction depends on INH, U1 EN and Q1 (tested by LM-13); IMON itself by LM-70.	PCB-202, SUP-314, SUP-417, BLD-401, BLD-402, BLD-403, PCB-303	6	PROVISIONAL	OQ-044
SM-72	Prevents violation	U2 cycle-by-cycle current limit and hiccup: a hard 12 V short collapses the rail and the power into the short stays at a few watts	HW in U2 (TI)	Power supply: current control of the output (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	Credited only on the 12 V rows defined as hard (below the hiccup entry). The limit and hiccup entry level are not characterised against a partly resistive short, and U2's FMEDA is on request (OQ-007): Medium. A loss of the limit is latent with no test (F07-063).	BCK-102, BCK-104, BCK-403	2	GATED	OQ-007
SM-73	Prevents violation	Vehicle feed fuse at J3/J4 clears a hard short ahead of the U1 sense (assumption of use)	Off-board (vehicle harness fuse, A-09); SUP-220 action asks for a dedicated fuse per corner sized for a C7-class short	Power supply: current control of the input, off-board (Low)	60% ASSUMED	60% ASSUMED	The only limit ahead of R7. Rating and clearing time are not specified (OQ-025): a short between the corner's peak draw and the fuse's fast-clear current heats the input copper, J3/J4, L1 and Q1 for seconds or more, and a fuse shared by several corners is sized above one corner's short. The Low ceiling is argued only because the rows credited are metallic shorts ahead of R7 (TVS junction, pad bridge, hard capacitor short), which draw the battery's short-circuit current far above any feed-fuse rating; the SUP-220 action (dedicated, sized fuse) is what would justify more.	SUP-220, SUP-108, PCB-302, PCB-507	4	NO-CLIENT-DATA	OQ-025
LM-01	Detects latent	DRVOFF path test at power-up and before each EPB operation (float and drive DRVOFF, read STATUS2.DRV_STAT)	SW	Test pattern of the shut-off path at start-up (Medium)	90% ASSUMED	90% ASSUMED	Tests the pin, the pull-up and the U7 input once per operation	EPB-105, EPB-121	4	PROVISIONAL	OQ-032

ID	Kind	Mechanism	Implemented by	ISO 26262-5 Annex D basis	DC as built	DC with actions	Basis for the DC	DFMEA rows	Rows using it	Reason code	Closes with
LM-02	Detects latent	Current-sense path test (inrush plausibility at each commanded operation, key-on self-test)	SW	Plausibility of a sensor against a known stimulus (Medium)	90% ASSUMED	90% ASSUMED	A blind sense path shows no inrush at the next commanded operation	EPB-301, EPB-302, EPB-319	10	PROVISIONAL	OQ-032
LM-03	Detects latent	Periodic cut-off test (open Q11 with the bridge idle, confirm U7 VM undervoltage within 300 ms, close)	SW; cannot pass on VerB (R58 fitted), valid with actions	Test of the switch-off path at start-up or idle (Medium)	0% ASSUMED	**90% ASSUMED**	As built the cut-off is defeated by R58, so no test can show it works; with R58 not fitted the test covers Q11, R87, Q6 and CUTOFF1	EPB-401, EPB-411, EPB-412, EPB-413	6	PROVISIONAL	OQ-029
LM-04	Detects latent	MCU start-up self-tests (logic and memory BIST, error-module test)	HW and SW in U14 (TI)	Self-test by hardware at start-up (Medium to High)	90% ASSUMED	90% ASSUMED	TI's safety manual defines the tests and their coverage; not public	MCU-504, MCU-505, MCU-506	6	GATED	OQ-007
LM-05	Detects latent	PMIC start-up self-test and test of the reset and safe-state outputs	HW in U3 (TI) and SW	Self-test by hardware at start-up; test of the reset path (Medium)	90% ASSUMED	90% ASSUMED	TI's PMIC safety manual defines the BIST coverage; the reset-path test is a software requirement	PMC-211, PMC-404, EPB-408	15	GATED	OQ-007
LM-06	Detects latent	U7 status byte, DEVICE_ID and nFAULT/FAULT consistency on every access	SW	Information redundancy on the interface (Medium)	90% ASSUMED	90% ASSUMED	A dead or corrupted readback fails the fixed status bits on the next access	EPB-507, EPB-509, EPB-514	8	PROVISIONAL	OQ-032
LM-07	Detects latent	U7 off-state diagnostics (open load and terminal shorts) run periodically in standby	SW (U7 feature, disabled by default)	Periodic test of outputs (Low)	60% ASSUMED	60% ASSUMED	Detects OUTx shorts to VM or GND at rest; not every harness short	EPB-314, EPB-206	2	PROVISIONAL	OQ-032
LM-08	Detects latent	End-to-end protection of the vehicle-speed message (CRC, alive counter, timeout) checked by U14	SW (AUTOSAR E2E or equivalent)	Communication bus: information redundancy combined with frame counter and timeout monitoring (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	The profile and data ID of the speed message are not specified yet; credited at Medium until they are	MCU-508, CAN-101	1	PROVISIONAL	OQ-038
LM-10	Detects latent	U5 analog built-in self-test (ABIST) at every start-up, result checked over SPI before the drive is enabled	HW in U5 (TI) and SW	Self-test by hardware at start-up (Low to Medium)	60% ASSUMED	60% ASSUMED	Coverage of the VDS and Rsense comparators and of nFAULT by ABIST is not published (OQ-007); credited Low	BLD-215, BLD-226	1	GATED	OQ-007
LM-11	Detects latent	U5 DRVOFF and nSLEEP path test at power-up and before each drive enable (assert each, command a low-side pulse, confirm no phase current and the U5 status), with the U14 GPIOs first left as inputs	SW	Test pattern of the shut-off path at start-up (Medium)	90% ASSUMED	90% ASSUMED	The test exercises the whole path (U14 pin, net, U5 input, gate outputs) and checks the result by phase current, so the Medium ceiling is argued; it runs once per drive enable	BLD-102, BLD-103, BLD-105	3	PROVISIONAL	OQ-032
LM-12	Detects latent	Angle channel compare seen from the monitor channel (a U13 or channel-2 fault shows as a mismatch at the next movement)	SW (same software as SM-14)	Comparison of redundant sensors (High claimable)	90% ASSUMED	**97% ASSUMED**	Same detection and same limits as SM-14, applied to the channel that is not used for commutation	ANG-201, ANG-309	4	PROVISIONAL	OQ-038
LM-13	Detects latent	Supply cut-off test (key-off drop of INH with the bridges off, confirm DC_BUS decays and U14 loses power within 10 ms; CMPSS VMON trip checked by DAC-code shift at start-up)	SW	Test of the switch-off path at shut-down (Low to Medium)	60% ASSUMED	60% ASSUMED	Tests U1, Q1 and both INH paths once per drive cycle; does not test the VMON divider scale, and the cut-off is not latched (OQ-041)	SUP-208, CAN-408, SUP-404	14	PROVISIONAL	OQ-014
LM-14	Detects latent	Pedal fall-back input plausibility (valid band with rail bands reserved, SENT CRC and timeout, force-versus-travel, released-zero check at key-on)	SW	Plausibility check of redundant sensors (Low to Medium)	60% ASSUMED	60% ASSUMED	The force-travel relation depends on the pedal feel simulator and catches only large errors; an open wire reads just above the valid band (PED-104, PED-302)	PED-302, PED-104, PED-216	2	PROVISIONAL	OQ-009
LM-15	Detects latent	Phase-isolation test at each start-up (each switch opened in turn, a low-side pulse applied, no current allowed)	SW; with actions only	Test of the switch-off path at start-up (Medium)	0% ASSUMED	**90% ASSUMED**	Tests each switch of the isolation individually by its effect on current, so the Medium ceiling is argued	BLD-201	1	PROVISIONAL	OQ-032
LM-20	Detects latent	U6 SPI communication check: fixed field and idle level of every WSS001 response; a failed check marks the speed invalid	SW in U14	Information redundancy on the interface (Low)	60% ASSUMED	60% ASSUMED	A dead or stuck SDO is seen only if the WSS001 frame has fixed bits or a CRC, which is unknown (OQ-008), and the SDOEPB idle level is undefined on VerB (WSS-314). Low until the frame format is known.	WSS-314, EPB-509	2	UNRELEASED	OQ-008
LM-40	Detects latent	End-to-end protection and timeout of the corner's EPB status message, checked by the brake controller; a failed check or timeout is treated as 'EPB hold unavailable at this corner' (other corner re-clamps, driver warned)	SW in U14 (sender) and the brake controller (receiver); assumption of use	Communication bus: information redundancy with frame counter and timeout monitoring (High claimable; Medium credited)	90% ASSUMED	90% ASSUMED	Detects a corrupted or missing status from this corner, which would otherwise hide a hold loss from the other corner and the driver. The profile and timeout are not specified, so Medium is credited, as for SM-24. The DFMEA has no row for the EPB status path; EPB-510 and EPB-505 only require the report.	EPB-505, EPB-510, MCU-508	1	PROVISIONAL	OQ-040
LM-70	Detects latent	IMON path plausibility: at each commanded BLDC or EPB actuation IMON must rise with the phase-shunt sum (and the EPB current) within tolerance; offset checked at key-on with the bridges idle	Not on VerB; with actions: SW in U14	Plausibility of a sensor against a known stimulus (Medium)	0% ASSUMED	**90% ASSUMED**	Same argument as LM-02: a stuck or scaled IMON fails the next actuation, which gives a stimulus of several amps. Medium ceiling argued because every drive cycle actuates the brake many times.	SUP-314, SUP-322, PCB-202	1	PROVISIONAL	OQ-032

Annex D sets the maximum coverage a technique can claim (Low 60 %, Medium 90 %, High 99 %). The claimed values are at or below those levels and must be shown by the verification named in the DFMEA row.

FIT data: base failure rates and failure-mode splits

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

Vehicle operating lifetime for the dual-point PMHF term (h) **8,000 ASSUMED**

FIT key	Description	Parts	λ (FIT)	Source or basis	Failure-mode split	Reason code	Closes with
U14	MCU F29P329SM-Q1 (whole device)	U14	150.0 ASSUMED	Order of magnitude for a large automotive MCU with flash, before safety mechanisms	Per row on the goal tabs (TI FMEDA not public)	GATED	OQ-007
U7	EPB H-bridge driver DRV8263-Q1	U7	20.0 ASSUMED	Order of magnitude for a 65 V H-bridge driver	Per row on the goal tabs (TI FS document on request)	GATED	OQ-007
U3	Safety PMIC TPS653860-Q1	U3	40.0 ASSUMED	Order of magnitude for a multi-rail safety PMIC	Per row on the goal tabs (TI FMEDA on request)	GATED	OQ-007
U5	BLDC gate driver DRV3263-Q1	U5	30.0 ASSUMED	Order of magnitude for a three-phase gate driver	Per row on the goal tabs (TI safety manual under NDA)	GATED	OQ-007
U6	Wheel-speed interface WSS001-Q1	U6	15.0 ASSUMED	Order of magnitude for a wheel-speed interface IC	Per row on the goal tabs (no public datasheet)	UNRELEASED	OQ-008
FET-80V	Power MOSFET 80 V (SQJA90EP)	Q1, Q2, Q4, Q5, Q7-Q11	10.0 ASSUMED	Order of magnitude under motor-drive stress; no vendor FIT for ISO 26262 use	D-S short 40 %, D-S open 20 %, G-S short 15 %, on-resistance increase 25 %	JUDGMENT	OQ-010
DTR	Dual digital transistor (BCR22PN)	Q6	2.0 ASSUMED	SN 29500-order value for a small-signal transistor pair	C-E short 40 %, open 40 %, gain drift 20 %	NO-CLIENT-DATA	OQ-010
RES-0402	Thick-film chip resistor 0402	R84-R96, R133, R135, R137, new resistors	0.3 ASSUMED	SN 29500-order value	Open 60 %, short 10 %, drift 30 %	NO-CLIENT-DATA	OQ-010
RES-0R	Zero-ohm link 0402	R38, R57, R58	0.1 ASSUMED	SN 29500-order value	Open 100 % (no other credible mode)	NO-CLIENT-DATA	OQ-010
MLCC-0402	MLCC 0402, 50 V	C88-C94, C98, C99, C100	0.5 ASSUMED	SN 29500-order value	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-010
MLCC-0603	MLCC 0603, 100 V soft termination	C97	0.8 ASSUMED	SN 29500-order value	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-010
MLCC-1210	MLCC 1210, 100 V general grade	C96	2.0 ASSUMED	SN 29500-order value raised for flex-crack exposure (DFMEA PCB-201)	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-010
DIODE-SS	Small-signal Schottky diode (BAT46W)	D12	1.0 ASSUMED	SN 29500-order value	Short 50 %, open 30 %, leakage 20 %	NO-CLIENT-DATA	OQ-010
PAD	Wire pad and solder joint (one pad)	J1, J2, J5, J6	0.5 ASSUMED	SN 29500-order value for a soldered connection under vibration	Open 70 %, short to adjacent pad or harness 30 %	NO-CLIENT-DATA	OQ-010
MLCC-0603G	MLCC 0603, 25-50 V general	C63, C67, C95, R53	0.5 ASSUMED	SN 29500-order value	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-010
U4	1.25 V core buck TPS62902-Q1	U4	12.0 ASSUMED	TI SFFS465A Table 2-1, IEC TR 62380 / ISO 26262-11 at the 0.5 W column (die 8 + package 4); column chosen by sev10	TI SFFS465A: output out of spec 22 %, HS or LS FET stuck on 20 %, power FET damage 36 %, PG 13 %, EN 9 %	JUDGMENT	OQ-010
U2	12 V buck LM68645-Q1	U2	20.0 ASSUMED	Order of magnitude for a 65 V synchronous buck	Per row on the goal tabs (TI FMEDA on request)	GATED	OQ-007
U1	Ideal diode and surge stopper LM74930-Q1	U1	14.0	TI SFFS950 Table 2-1, IEC TR 62380 / ISO 26262-11 motor-control profile, 42 mW (die 3 + package 11)	TI SFFS950 section 3 (gate drives, IMON, OCP, SCP, UV/OV, pin shorts)		
Y1	MCU clock CDC6C-Q1 (BAW oscillator)	Y1	3.0	TI SFFS685 section 2.4, DLY package (die 2 + package 1)	TI SFFS685: clock degraded 40 %, wrong frequency 30 %, no clock 30 %		
TCAN	CAN FD transceiver TCAN1043H-Q1 (VSON)	U8, U10	9.0	TI SLLA525A Table 2-1, IEC TR 62380 / ISO 26262-11 motor-control profile, 126 mW (die 3 + package 6)	TI SLLA525A: receiver 35 %, transmitter 35 %, stuck in sleep 15 %, bus dominant 5 %, pin short 5 %, false fault report 5 %		
U12-U13	Angle sensor TMAG6180-Q1	U12, U13	10.0 ASSUMED	Order of magnitude for an analog Hall/AMR angle sensor (reference.yaml)	Per row on the goal tabs (TI FS manual TMAG618X-Q1-FS on request)	GATED	OQ-007
SHUNT	Metal-element current shunt 0.5 mOhm (BVN-Z)	R61, R80, R81	1.0 ASSUMED	SN 29500-order value for a metal-strip resistor	Open 30 %, resistance drift 70 % (no credible short)	NO-CLIENT-DATA	OQ-010
U5-PAS	U5 support passives (C62, C64, C65, C67, C69, C72, C77, R64, R65, R68, R59, R62, R141, R143), summed	14 parts	5.6 ASSUMED	Sum of class values: 7 MLCC 0603 25 V at 0.5 (MLCC-0603G), 3 resistors 0603 at 0.3, 4 resistors 0402 at 0.3	Per row (aggregated; all modes safe for SG-01)	NO-CLIENT-DATA	OQ-010
BUS-CAP	48V/12V_P bus capacitors (C60, C73, C74 330 uF aluminium; C61, C75, C76 4.7 uF 1210; C68 1 uF 1206), summed	7 parts	16.0 ASSUMED	Sum of class values: 3 aluminium electrolytics at 3 FIT, 3 MLCC 1210 at 2 (MLCC-1210), 1 MLCC 1206 at 1	Per row (aggregated)	NO-CLIENT-DATA	OQ-010
CSA-FE	Phase-current sense front end (R60, R63, R78, R79, R82, R83, R71, R76, R77; C66, C70, C71, C78-C82, C84-C87), summed	20 parts	8.2 ASSUMED	Sum of class values: 9 resistors 0402 at 0.3, 11 MLCC 0402 at 0.5	Reading error 70 %, no effect 30 % (aggregated)	NO-CLIENT-DATA	OQ-010
ADCREF-FE	ADC reference network (L7, L8, L10 ferrites; C44, C83, C134 0402; C49, C116, C117 0603), summed	9 parts	5.4 ASSUMED	Sum of class values: 3 ferrite beads at 0.5, 3 MLCC 0402 at 0.5, 3 MLCC 0603 at 0.8	Reference lost (bead open, capacitor short) 50 %, other 50 % (aggregated)	NO-CLIENT-DATA	OQ-010
ANG-FE	Angle sensor front end, one channel (2 × 1 kOhm, 2 × 100 kOhm, 3 MLCC 0402, one 4-pin header J21 or J22), summed	8 parts per channel	3.7 ASSUMED	Sum of class values: 4 resistors 0402 at 0.3, 3 MLCC 0402 at 0.5, header 4 pins at 0.25	Signal error 70 %, other 30 % (aggregated)	NO-CLIENT-DATA	OQ-010

FIT key	Description	Parts	λ (FIT)	Source or basis	Failure-mode split	Reason code	Closes with
PED-FE	Pedal sensor input network, one channel (3 resistors 0402, 2 zero-ohm links, 2 MLCC 0402), summed	7 parts per channel	2.1 ASSUMED	Sum of class values: 3 × 0.3, 2 × 0.1 (RES-0R), 2 × 0.5	Value error 70 %, other 30 % (aggregated)	NO-CLIENT-DATA	OQ-010
INH-NET	Transceiver INH network (D6, D7 1N4148WS; R102, R112, R156, R19, R26, R36), summed	8 parts	3.8 ASSUMED	Sum of class values: 2 small-signal diodes at 1.0 (DIODE-SS), 6 resistors 0402 at 0.3	R156 open 5 %, other 95 % (aggregated)	NO-CLIENT-DATA	OQ-010
TVS-ESD	Dual ESD protection diode ESD2CAN24-Q1 (SOT-23)	D5	1.0 ASSUMED	SN 29500-order value for a TVS array (the value used for D5 inside WSS-FE)	Short 40 %, open 30 %, leakage or degraded clamp 30 %	NO-CLIENT-DATA	OQ-010
RAIL-DEC	Logic-rail decoupling capacitors (1.25V, 3.3V, 5V, 12V, 12V_Cobra, VCC_6V0), summed	47 parts: C57, C58, C123-C132; C37, C43, C48, C91, C98, C103, C107, C121, C122, C137-C147; C46, C51, C92, C101, C105; C27, C31-C36, C89; C25, C26, C30; C40, C41, C42, C56	31.3 ASSUMED	Sum of class values: 39 MLCC 0402 at 0.5 (MLCC-0402), 4 MLCC 0603 10 uF 10 V at 0.5 (MLCC-0603G), C26 0603 100 V at 0.8 (MLCC-0603), 7 MLCC 0805 22 uF general grade at 1.0 (no key yet; SN 29500-order, raised for flex exposure as PMC-103), C25 1210 at 2 (MLCC-1210). Parts inside ANG-FE (C109, C112) and ADCREF-FE (C44, C49, C83, C134) are excluded	Short 50 % (rail collapse), open or capacitance loss 50 % (class split of MLCC-0402)	NO-CLIENT-DATA	OQ-010
PWR-PASS	Supply-chain passives and small switches outside the rail decoupling (input stage, VSUP dropper, U1 and U2 support networks, 12 V switch, power inductors, PMIC and rail links), summed	D1, D3, D11, R99, C5-C10, C12, C16, C20-C24, C28, C29, C11, C13-C15, C17-C19, C115, C148, L1-L4, R7, Q3, Q12, R8-R17, R20, R21, R153, R24, R25, R27-R32, R154, R155, R23, R37, R38, R40-R43, R45, R49	45.0 ASSUMED	Sum of class values: D1 power TVS 2.0; D3, D11 at 1.0 (DIODE-SS); R99 0.3; 4 MLCC 1210 at 2 (C5, C6, C21, C22); 2 MLCC 1206 at 1 (C12, C16); 5 MLCC 0603 100 V at 0.8 (C7, C9, C10, C23, C24); 2 aluminium electrolytics at 3 (C8, C28); L1, L2 at 1.0, L3, L4 at 0.5; R7 at 1 (SHUNT); Q3, Q12 small-signal MOSFETs at 2 (as DTR); U1 support 11 resistors at 0.3, 2 links at 0.1, 9 MLCC 0402 at 0.5 (8.0); U2 support C20, C29 at 0.5, 7 resistors at 0.3, 3 links at 0.1 (3.4); PMIC links and series resistors 5 × 0.1 + 2 × 0.3 (1.1); R23, R38 links 0.2	Supply lost 44 % (TVS short 0.8, D3/D11/R99 open 0.78, capacitor shorts 7.0 + 1.8, inductors open 1.8, R7 open or high 0.65, Q3 open/G-S short/Rds and Q12 short 2.0, U1/U2/PMIC networks that trip or disable a supply 3.2 + 1.0 + 0.55, links 0.2: 19.8 of 45.0), other 56 %	NO-CLIENT-DATA	OQ-010
ALU-100V	Aluminium electrolytic 100 V SMD (EMVE, 100-330 uF), one part	C8, C28, C60, C73, C74	3.0 ASSUMED	SN 29500-order value for a wet aluminium electrolytic at 85 C board temperature, no ripple stress factor (the value inside BUS-CAP)	Short 20 %, open 30 %, capacitance loss or ESR rise 40 %, venting 10 %	NO-CLIENT-DATA	OQ-010
TVS-SMB	Power TVS diode SMBJ51CA (SMB, 600 W)	D1	2.0 ASSUMED	SN 29500-order value for a power suppressor diode; no AEC-Q101 statement for the fitted part (OQ-018)	Short 40 %, open 30 %, leakage or degraded clamp 30 % (as TVS-ESD)	NO-CLIENT-DATA	OQ-018
U1-NET	U1 current sense and OCP/SCP set network (R7 1 mOhm shunt; R11, R20, R21 0402; C14, C19 0402), summed	6 parts	2.9 ASSUMED	Sum of class values: R7 at 1 (SHUNT), 3 resistors at 0.3 (RES-0402; R11 is an ATC 504L thin-film part), 2 MLCC 0402 at 0.5	Disables OCP or SCP or raises its trip level 38 % (R11 open 0.18, R20 short 0.03, R21 short 0.03, C14 short 0.25, C19 short 0.25, R7 drift low 0.35 FIT; SUP-314), other 62 %	NO-CLIENT-DATA	OQ-010
BUS-MLCC	48V/12V_P bus MLCCs as built (C5, C6, C21, C22, C61, C75, C76 GRM 1210 100 V general grade; C23, C24 0603 100 V soft termination; C68 1206 100 V), summed	10 parts	16.6 ASSUMED	Sum of class values: 7 × 2 (MLCC-1210, raised for flex-crack exposure), 2 × 0.8 (MLCC-0603), 1 × 1 (1206 100 V AEC-Q200, as in BUS-CAP)	Short 50 % (hard or resistive per row), open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-018
BUS-MLCC-B	48V/12V_P bus MLCCs with the DFMEA actions (the seven 1210 parts replaced by AEC-Q200 soft-termination 100 V parts away from the outline; C23, C24, C68 unchanged), summed	10 parts	9.6 ASSUMED	Sum of class values: 7 × 1 (1210 AEC-Q200 soft termination: the SN 29500-order value without the flex-crack raise of MLCC-1210), 2 × 0.8, 1 × 1	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-018
BDC-MLCC	48V/12V_BDC EPB bulk as built (C96 GRM 1210 100 V general grade; C97 0603 100 V soft termination), summed	C96, C97	2.8 ASSUMED	Sum of class values: 2 (MLCC-1210) + 0.8 (MLCC-0603)	Short 50 % (hard or resistive per row), open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-018
BDC-MLCC-B	48V/12V_BDC EPB bulk with the DFMEA actions (C96 AEC-Q200 soft termination, 10 mm from the edge; C97 unchanged), summed	C96, C97	1.8 ASSUMED	Sum of class values: 1 (1210 AEC-Q200 soft termination) + 0.8 (MLCC-0603)	Short 50 %, open 30 %, capacitance loss 20 %	NO-CLIENT-DATA	OQ-018
CAP-12V	12 V rail capacitors as built (C25 GRM 1210; C27, C31-C33 GRM21BR61E226ME44 22 uF 25 V X5R 0805, rated to 85 C; C26 0603; C34-C36, C89 0402; C62 0603 25 V), summed	11 parts	13.3 ASSUMED	Sum of class values: C25 2 (MLCC-1210); C27, C31-C33 4 × 2 (SN 29500-order 1 FIT doubled for operation above the 85 C rating at the assumed 105 C board, BCK-409); C26 0.8 (MLCC-0603); 4 × 0.5 (MLCC-0402); C62 0.5 (MLCC-0603G)	Short 50 % (hard or resistive per row), open or capacitance loss 50 %	NO-CLIENT-DATA	OQ-010
CAP-12V-B	12 V rail capacitors with the DFMEA actions (C25 AEC-Q200 soft termination; C27, C31-C33 AEC-Q200 X7R >= 50 V, 125 C; others unchanged), summed	11 parts	6.3 ASSUMED	Sum of class values: C25 1; 4 × 0.5 (automotive X7R within its temperature rating, as MLCC-0603G); C26 0.8; 4 × 0.5; C62 0.5	Short 50 %, open or capacitance loss 50 %	NO-CLIENT-DATA	OQ-010

FIT key	Description	Parts	λ (FIT)	Source or basis	Failure-mode split	Reason code	Closes with
CAF-48V	CAF path from one 48 V-class net to GND inside the board, as built (0.40-0.53 mm inner spacing and hole-wall-to-plane, FR-4 without CAF grade, uncoated), per net pair	!PCB1 (48V/12V_IN, 48V/12V_IN_FILTERED, NetC7_2, NetQ2_5, 48V/12V_P, 48V/12V_BDC, SHA, SHB, SHC to GND)	1.0 ASSUMED	No handbook value for CAF. DFMEA PCB-302/PCB-303 rate O 4, which scales.yaml anchors at 1-10 FIT for the whole row; 1 FIT per net pair puts the nine pairs at the upper part of that band	Resistive path 100 % (PCB-303: resistive long before it becomes a hard short)	JUDGMENT	OQ-016
CAF-48V-R	CAF path from one 48 V-class net to GND with the DFMEA actions (CAF-resistant laminate by IPC-4101 slash sheet, >= 0.5 mm inner spacing and hole-wall-to-plane), per net pair	!PCB1 (same nine net pairs)	0.2 ASSUMED	DFMEA after-occurrence O 2 (< 1 FIT per row, scales.yaml); a fifth of the as-built value per net pair	Resistive path 100 %	JUDGMENT	OQ-016
WSS-FE	Wheel-speed front end (D5, R84, R86, R88, C88, C90, C93, C94, C95, J1, J2), summed	11 parts	5.4 ASSUMED	Sum of the class values above: 3 resistors 0.9, 5 MLCC 2.5, TVS 1.0, 2 pads 1.0	Loss of pulses 60 %, other 40 % (aggregated, detailed on the SG-05 tab)	NO-CLIENT-DATA	OQ-010

Values with a blank reason code are quoted from TI FIT/FMD documents (U1, U8/U10, Y1). The mission profile, temperature basis and handbook are on the Basis tab.

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Mission profile

Item	Value used	Basis	Status	Closes with
Board ambient temperature	−40 to +105 °C	OQ-010 working assumption. TI rates the reference design for −25 to 75 °C open-frame lab use only (TIDUFI0 Table 1-1).	ASSUMED (NO-CLIENT-DATA)	OQ-010
Service life	15 years	OQ-010 working assumption	ASSUMED (NO-CLIENT-DATA)	OQ-010
Operating hours over life	8,000 h	OQ-010 working assumption; used as the exposure time of latent faults in the dual-point PMHF term (FIT data tab, cell D3).	ASSUMED (NO-CLIENT-DATA)	OQ-010
Temperature for passive failure rates	85 °C board	sev10 choice inside the assumed range; no temperature or electrical stress factors applied yet.	ASSUMED (NO-CLIENT-DATA)	OQ-010

Failure-rate sources, by component class

Class	Source used in Rev A	Rev B plan	Status	Closes with
TI ICs with a published FIT/FMD document (U1, U4, U8, U10, Y1)	TI document as written: IEC TR 62380 / ISO 26262-11 basis, TI's motor-control mission profile, die and package rates summed	Rescale to the Quillon Motors mission profile once it is set	Sourced (U4 column choice: JUDGMENT)	OQ-010
TI ICs whose data is on request (U14, U3, U5, U7, U2)	Order-of-magnitude rate per device; failure-mode shares per row set by sev10	TI FMEDA and safety manual per device: FIT, failure-mode distribution and on-chip diagnostic coverage	ASSUMED (GATED)	OQ-007
WSS001-Q1 (U6)	Order-of-magnitude rate; shares set by sev10	Device documentation	ASSUMED (UNRELEASED)	OQ-008
Passives, discrete semiconductors, solder joints	SN 29500-order class values at 85 °C, no stress factors; typical class failure-mode splits	SN 29500 or IEC 61709 with temperature and stress factors from the mission profile; splits cited from FMD-2016	ASSUMED (NO-CLIENT-DATA, JUDGMENT)	OQ-010
Transient (soft-error) faults	Not counted in Rev A: the MCU soft-error rate comes with TI's FMEDA	Listed separately and counted in SPFM and PMHF, not in LFM (ISO 26262-5)	Open	OQ-007

Targets (ISO 26262-5:2018 Tables 4, 5 and 6)

ASIL	SPFM	LFM	PMHF	Nature
D	≥ 99%	≥ 90%	< 10 FIT	Required
C	≥ 97%	≥ 80%	< 100 FIT	Required
B	≥ 90%	≥ 60%	< 100 FIT	Recommended

A	—	—	—	No hardware metric targets

The PMHF targets apply to the whole item for each safety goal. The corner ECU's share is not yet allocated (OQ-046); with two EPB corners and four brake corners per vehicle, the per-corner value must be multiplied accordingly before it is compared.

Equations and conventions

Quantity	Definition	Convention in this workbook
λ counted	Σ λ mode over rows whose class is not n/a	IC functions that cannot affect the goal are n/a, not Safe, so they do not inflate the metrics
SPFM	1 − Σ(λ SPF + λ RF) / Σλ counted	Safe faults stay in the denominator (Annex C)
LFM	1 − Σλ MPF,latent / (Σλ counted − Σλ SPF − Σλ RF)	A fault is Latent only if it disables a mechanism that is active in that scenario
PMHF	$\Sigma\lambda$ SPF + $\Sigma\lambda$ RF + $\Sigma(\lambda$ MPF,latent × partner $\lambda \times T)/10^9$	Partner λ = the faults the lost mechanism controls (listed per row). T = operating hours over life. No ½ factor (conservative); the exposure of detected dual-point faults over their test interval is neglected
Diagnostic coverage	Annex D: Low 60 %, Medium 90 %, High 99 %	Band values are maximums; each claim needs the verification named in its DFMEA row
Credit for a mechanism	It must detect the fault and reach the safe state within the FTTI	Where a reaction only stops an actuator (SG-03 cut-off), the credit is conditional (OQ-047)

sev10

Dependent-failure note: shared causes that the metrics do not see

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SPFM, LFM and PMHF assume independent random faults. These are the places where one cause can defeat a function and its safety mechanism together (ISO 26262-9 clause 7). Each has a disposition; a full dependent-failure analysis follows in the technical safety concept.

#	Shared cause or element	Mechanism at risk	Goals	Disposition	DFMEA rows	Status
1	Both lockstep cores and the MCU I/O share one supply (U4 1.25 V core, U3 LDO1 3.3 V)	SM-01 (lockstep)	SG-01, SG-02, SG-03	Covered by SM-08: the PMIC monitors the core rail through EXT_VMON1 in a separate die. LDO1's monitor shares its die with the regulator (Medium credit). Thresholds in PMIC NVM (OQ-002).	MCU-507, PMC-303, PMC-304	Open (OQ-002)
2	U7 input logic fault and its reaction (DRVOFF) in the same die	SM-03 as built	SG-03	As built: Low coverage only. With the actions the reaction opens Q11 or puts U7 to sleep through SAFE_OUT1, both outside U7.	EPB-103, EPB-408	Closed by actions
3	U14 both commands the EPB and runs the software mechanisms (SM-03 to SM-07, LM-01 to LM-08)	All SW mechanisms	SG-03	Faults in the U14 CPU are covered by SM-01 and the PMIC reset path (different die). Port faults: detection in software, reaction through Q11 or SAFE_OUT1 on different pins and peripherals than the stuck ones. Freedom from interference for the software: ISO 26262-6.	EPB-101, MCU-513	Open: pin and peripheral independence to be shown
4	Shared SPI-D bus between U6 (wheel speed) and U7 (EPB)	SM-05, SM-07	SG-03, SG-05	Standstill is taken from WSSO pulse timing and the other wheels over CAN, never from SPI data; U7 configuration is locked and read back cyclically.	EPB-519, EPB-502	Requirement in the TSC
5	5 V LDO2 feeds U6 and both CAN transceivers	SM-07	SG-03, SG-05	Loss of 5 V removes the pulses and the independent speed together. The rule 'loss of pulses is invalid, never standstill' is local and needs neither; EPB static apply inhibited on loss of both buses.	PMC-207	Requirement in the TSC
6	Y1 clocks U14, so it times the wheel-speed capture and the command sequence	SM-07	SG-03, SG-05	The PMIC Q&A watchdog runs on its own oscillator and breaks its window on a U14 frequency error (SM-02).	MCU-203	Covered
7	A 48 V bus short at the H-bridge overstresses the Q11 gate	SM-03, SM-04 reaction	SG-03, SG-07	The same event that shorts the bus can rupture the Q11 gate oxide, leaving the cut-off unable to open. Branch current limit and a gate-source clamp are DFMEA actions.	EPB-201, EPB-417, EPB-423	Open (DFMEA actions)
8	External surge or load dump through the supply input	U1, SM-09	All	Not a random hardware fault of the ECU: U1 overvoltage cut-off and the CMPSS window (SM-09) remove 48V/12V_P. Coupling faults (common supply to U3, U5, U7) are listed here, not in the metrics.	SUP-102, SUP-304, PMC-102	Open (OQ-014, OQ-017)
9	EMC coupling onto the long SPI-D stubs	SM-05	SG-03	Cyclic readback of U7 configuration and the register lock; the frame has no CRC.	EPB-502	Covered (PROVISIONAL)
10	Board-level thermal event near the EPB stage (C96 crack short)	EPB stop paths	SG-03, SG-07	Removes the EPB supply (safe for SG-03); its thermal risk is counted on SG-07.	PCB-202, EPB-201	Counted on SG-07
11	The Q11 cut-off serves opposite goals: it stops an unintended apply (SG-03) and an unintended release (SG-04), but once open it removes the only way to re-clamp this corner	SM-03, SM-04, LM-03	SG-03, SG-04	Any opening at standstill (a false trip, the LM-03 test) leaves the hold with no re-apply at this corner. LM-03 must run only with both rear EPBs applied; the reaction when standstill cannot be confirmed is for the client.	EPB-409, EPB-411	Open (OQ-053)

#	Shared cause or element	Mechanism at risk	Goals	Disposition	DFMEA rows	Status
12	Systematic thermal chains outside the random-fault rows: D1 conducting near 60 V, Q11 in linear mode as built, Q6 at 58-66 V, 25 V capacitors at 105 °C, aluminium wear-out, Q1 start-up SOA, the R22 variant, C8 under reverse polarity, shared assembly stress of the 1210 MLCCs, surface leakage across bare 48 V gaps	SM-70 to SM-73	SG-07	Design deficiencies, not random faults: corrected by the DFMEA actions, not by a safety mechanism. Listed so the SG-07 metrics are not read as covering them.	SUP-101, EPB-402, EPB-405, BCK-409, BLD-404, SUP-201, BCK-402, SUP-104, PCB-101	Open (DFMEA actions; OQ-011, OQ-017, OQ-029, OQ-030)

sev10 — Assumptions register: every ASSUMED value in this workbook

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393 assumed values. Reason codes: GATED (TI data on request), UNRELEASED (no public device data), NO-CLIENT-DATA (mission profile or allocation not supplied), JUDGMENT (sev10 judgment), PROVISIONAL (software mechanism not yet specified in detail).

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
1	FIT data	Lifetime (h)	NO-CLIENT-DATA	Vehicle operating hours for the dual-point term	OQ-010	Client data
2	Summary	PMHF target	NO-CLIENT-DATA	Corner ECU compared with the item-level target	OQ-046	Client data
3	FIT data	U14	GATED	TI supplies this data on request only. Order of magnitude for a large automotive MCU with flash, before safety mechanisms.	OQ-007	TI data
4	FIT data	U7	GATED	TI supplies this data on request only. Order of magnitude for a 65 V H-bridge driver.	OQ-007	TI data
5	FIT data	U3	GATED	TI supplies this data on request only. Order of magnitude for a multi-rail safety PMIC.	OQ-007	TI data
6	FIT data	U5	GATED	TI supplies this data on request only. Order of magnitude for a three-phase gate driver.	OQ-007	TI data
7	FIT data	U6	UNRELEASED	The device has no public datasheet or safety data. Order of magnitude for a wheel-speed interface IC.	OQ-008	TI data
8	FIT data	FET-80V	JUDGMENT	Value set by sev10 engineering judgment. Order of magnitude under motor-drive stress; no vendor FIT for ISO 26262 use.	OQ-010	Client data
9	FIT data	DTR	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a small-signal transistor pair.	OQ-010	Client data
10	FIT data	RES-0402	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
11	FIT data	RES-0R	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
12	FIT data	MLCC-0402	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
13	FIT data	MLCC-0603	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
14	FIT data	MLCC-1210	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value raised for flex-crack exposure (DFMEA PCB-201).	OQ-010	Client data
15	FIT data	DIODE-SS	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
16	FIT data	PAD	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a soldered connection under vibration.	OQ-010	Client data
17	FIT data	MLCC-0603G	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value.	OQ-010	Client data
18	FIT data	U4	JUDGMENT	Value set by sev10 engineering judgment. TI SFFS465A Table 2-1, IEC TR 62380 / ISO 26262-11 at the 0.5 W column (die 8 + package 4); column chosen by sev10.	OQ-010	Client data
19	FIT data	U2	GATED	TI supplies this data on request only. Order of magnitude for a 65 V synchronous buck.	OQ-007	TI data
20	FIT data	U12-U13	GATED	TI supplies this data on request only. Order of magnitude for an analog Hall/AMR angle sensor (reference.yaml).	OQ-007	TI data
21	FIT data	SHUNT	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a metal-strip resistor.	OQ-010	Client data
22	FIT data	U5-PAS	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 7 MLCC 0603 25 V at 0.5 (MLCC-0603G), 3 resistors 0603 at 0.3, 4 resistors 0402 at 0.3.	OQ-010	Client data
23	FIT data	BUS-CAP	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 3 aluminium electrolytics at 3 FIT, 3 MLCC 1210 at 2 (MLCC-1210), 1 MLCC 1206 at 1.	OQ-010	Client data
24	FIT data	CSA-FE	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 9 resistors 0402 at 0.3, 11 MLCC 0402 at 0.5.	OQ-010	Client data
25	FIT data	ADCREF-FE	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 3 ferrite beads at 0.5, 3 MLCC 0402 at 0.5, 3 MLCC 0603 at 0.8.	OQ-010	Client data
26	FIT data	ANG-FE	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 4 resistors 0402 at 0.3, 3 MLCC 0402 at 0.5, header 4 pins at 0.25.	OQ-010	Client data
27	FIT data	PED-FE	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 3 × 0.3, 2 × 0.1 (RES-0R), 2 × 0.5.	OQ-010	Client data
28	FIT data	INH-NET	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 2 small-signal diodes at 1.0 (DIODE-SS), 6 resistors 0402 at 0.3.	OQ-010	Client data
29	FIT data	TVS-ESD	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a TVS array (the value used for D5 inside WSS-FE).	OQ-010	Client data
30	FIT data	RAIL-DEC	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 39 MLCC 0402 at 0.5 (MLCC-0402), 4 MLCC 0603 10 uF 10 V at 0.5 (MLCC-0603G), C26 0603 100 V at 0.8 (MLCC-0603), 7 MLCC 0805 22 uF general grade at 1.0 (no key yet; SN 29500-order, raised for flex exposure as PMC-103), C25 1210 at 2 (MLCC-1210). Parts inside ANG-FE (C109, C112) and ADCREF-FE (C44, C49, C83, C134) are excluded.	OQ-010	Client data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
31	FIT data	PWR-PASS	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: D1 power TVS 2.0; D3, D11 at 1.0 (DIODE-SS); R99 0.3; 4 MLCC 1210 at 2 (C5, C6, C21, C22); 2 MLCC 1206 at 1 (C12, C16); 5 MLCC 0603 100 V at 0.8 (C7, C9, C10, C23, C24); 2 aluminium electrolytics at 3 (C8, C28); L1, L2 at 1.0, L3, L4 at 0.5; R7 at 1 (SHUNT); Q3, Q12 small-signal MOSFETs at 2 (as DTR); U1 support 11 resistors at 0.3, 2 links at 0.1, 9 MLCC 0402 at 0.5 (8.0); U2 support C20, C29 at 0.5, 7 resistors at 0.3, 3 links at 0.1 (3.4); PMIC links and series resistors 5 × 0.1 + 2 × 0.3 (1.1); R23, R38 links 0.2.	OQ-010	Client data
32	FIT data	ALU-100V	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a wet aluminium electrolytic at 85 C board temperature, no ripple stress factor (the value inside BUS-CAP).	OQ-010	Client data
33	FIT data	TVS-SMB	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. SN 29500-order value for a power suppressor diode; no AEC-Q101 statement for the fitted part (OQ-018).	OQ-018	Client data
34	FIT data	U1-NET	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: R7 at 1 (SHUNT), 3 resistors at 0.3 (RES-0402; R11 is an ATC 504L thin-film part), 2 MLCC 0402 at 0.5.	OQ-010	Client data
35	FIT data	BUS-MLCC	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 7 × 2 (MLCC-1210, raised for flex-crack exposure), 2 × 0.8 (MLCC-0603), 1 × 1 (1206 100 V AEC-Q200, as in BUS-CAP).	OQ-018	Client data
36	FIT data	BUS-MLCC-B	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 7 × 1 (1210 AEC-Q200 soft termination: the SN 29500-order value without the flex-crack raise of MLCC-1210), 2 × 0.8, 1 × 1.	OQ-018	Client data
37	FIT data	BDC-MLCC	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 2 (MLCC-1210) + 0.8 (MLCC-0603).	OQ-018	Client data
38	FIT data	BDC-MLCC-B	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: 1 (1210 AEC-Q200 soft termination) + 0.8 (MLCC-0603).	OQ-018	Client data
39	FIT data	CAP-12V	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: C25 2 (MLCC-1210); C27, C31-C33 4 × 2 (SN 29500-order 1 FIT doubled for operation above the 85 C rating at the assumed 105 C board, BCK-409); C26 0.8 (MLCC-0603); 4 × 0.5 (MLCC-0402); C62 0.5 (MLCC-0603G).	OQ-010	Client data
40	FIT data	CAP-12V-B	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of class values: C25 1; 4 × 0.5 (automotive X7R within its temperature rating, as MLCC-0603G); C26 0.8; 4 × 0.5; C62 0.5.	OQ-010	Client data
41	FIT data	CAF-48V	JUDGMENT	Value set by sev10 engineering judgment. No handbook value for CAF. DFMEA PCB-302/PCB-303 rate O 4, which scales.yaml anchors at 1-10 FIT for the whole row; 1 FIT per net pair puts the nine pairs at the upper part of that band.	OQ-016	Client data
42	FIT data	CAF-48V-R	JUDGMENT	Value set by sev10 engineering judgment. DFMEA after-occurrence O 2 (< 1 FIT per row, scales.yaml); a fifth of the as-built value per net pair.	OQ-016	Client data
43	FIT data	WSS-FE	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. Sum of the class values above: 3 resistors 0.9, 5 MLCC 2.5, TVS 1.0, 2 pads 1.0.	OQ-010	Client data
44	FIT data	FET-80V split	JUDGMENT	Class failure-mode split: D-S short 40 %, D-S open 20 %, G-S short 15 %, on-resistance increase 25 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
45	FIT data	DTR split	JUDGMENT	Class failure-mode split: C-E short 40 %, open 40 %, gain drift 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
46	FIT data	RES-0402 split	JUDGMENT	Class failure-mode split: Open 60 %, short 10 %, drift 30 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
47	FIT data	RES-0R split	JUDGMENT	Class failure-mode split: Open 100 % (no other credible mode). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
48	FIT data	MLCC-0402 split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
49	FIT data	MLCC-0603 split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
50	FIT data	MLCC-1210 split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
51	FIT data	DIODE-SS split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, leakage 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
52	FIT data	PAD split	JUDGMENT	Class failure-mode split: Open 70 %, short to adjacent pad or harness 30 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
53	FIT data	MLCC-0603G split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment

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54	FIT data	SHUNT split	JUDGMENT	Class failure-mode split: Open 30 %, resistance drift 70 % (no credible short). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
55	FIT data	U5-PAS split	JUDGMENT	Class failure-mode split: Per row (aggregated; all modes safe for SG-01). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
56	FIT data	BUS-CAP split	JUDGMENT	Class failure-mode split: Per row (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
57	FIT data	CSA-FE split	JUDGMENT	Class failure-mode split: Reading error 70 %, no effect 30 % (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
58	FIT data	ADCREF-FE split	JUDGMENT	Class failure-mode split: Reference lost (bead open, capacitor short) 50 %, other 50 % (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
59	FIT data	ANG-FE split	JUDGMENT	Class failure-mode split: Signal error 70 %, other 30 % (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
60	FIT data	PED-FE split	JUDGMENT	Class failure-mode split: Value error 70 %, other 30 % (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
61	FIT data	INH-NET split	JUDGMENT	Class failure-mode split: R156 open 5 %, other 95 % (aggregated). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
62	FIT data	TVS-ESD split	JUDGMENT	Class failure-mode split: Short 40 %, open 30 %, leakage or degraded clamp 30 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
63	FIT data	RAIL-DEC split	JUDGMENT	Class failure-mode split: Short 50 % (rail collapse), open or capacitance loss 50 % (class split of MLCC-0402). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
64	FIT data	PWR-PASS split	JUDGMENT	Class failure-mode split: Supply lost 44 % (TVS short 0.8, D3/D11/R99 open 0.78, capacitor shorts 7.0 + 1.8, inductors open 1.8, R7 open or high 0.65, Q3 open/G-S short/Rds and Q12 short 2.0, U1/U2/PMIC networks that trip or disable a supply 3.2 + 1.0 + 0.55, links 0.2: 19.8 of 45.0), other 56 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
65	FIT data	ALU-100V split	JUDGMENT	Class failure-mode split: Short 20 %, open 30 %, capacitance loss or ESR rise 40 %, venting 10 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
66	FIT data	TVS-SMB split	JUDGMENT	Class failure-mode split: Short 40 %, open 30 %, leakage or degraded clamp 30 % (as TVS-ESD). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
67	FIT data	U1-NET split	JUDGMENT	Class failure-mode split: Disables OCP or SCP or raises its trip level 38 % (R11 open 0.18, R20 short 0.03, R21 short 0.03, C14 short 0.25, C19 short 0.25, R7 drift low 0.35 FIT; SUP-314), other 62 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
68	FIT data	BUS-MLCC split	JUDGMENT	Class failure-mode split: Short 50 % (hard or resistive per row), open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
69	FIT data	BUS-MLCC-B split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
70	FIT data	BDC-MLCC split	JUDGMENT	Class failure-mode split: Short 50 % (hard or resistive per row), open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
71	FIT data	BDC-MLCC-B split	JUDGMENT	Class failure-mode split: Short 50 %, open 30 %, capacitance loss 20 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
72	FIT data	CAP-12V split	JUDGMENT	Class failure-mode split: Short 50 % (hard or resistive per row), open or capacitance loss 50 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
73	FIT data	CAP-12V-B split	JUDGMENT	Class failure-mode split: Short 50 %, open or capacitance loss 50 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
74	FIT data	CAF-48V split	JUDGMENT	Class failure-mode split: Resistive path 100 % (PCB-303: resistive long before it becomes a hard short). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
75	FIT data	CAF-48V-R split	JUDGMENT	Class failure-mode split: Resistive path 100 %. Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment
76	FIT data	WSS-FE split	JUDGMENT	Class failure-mode split: Loss of pulses 60 %, other 40 % (aggregated, detailed on the SG-05 tab). Typical published split for the part class; the handbook (FMD-2016 or IEC 61709) is still to be cited.	sev10	sev10 judgment

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
77	Safety mechanisms	SM-01 DC	GATED	TI supplies this data on request only. TI claims High coverage for the lockstep MCU; the value needs TI's safety manual and FMEDA.	OQ-007	TI data
78	Safety mechanisms	SM-02 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. A watchdog with its own time base is Medium at most (Annex D); the SAFE_OUT1 path the actions add improves the reaction, not the detection. As built the stop relies on the U7-internal DRVOFF pull-up.	OQ-002	TI data
79	Safety mechanisms	SM-03 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. As built the only reaction acts inside U7, the device that failed; with R58 not fitted the Q11 cut-off stops the bridge independently. Opening Q11 ends the apply but does not release the force built so far; the credit assumes the stop comes before that force is hazardous (EPB-409, OQ-047) For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052)..	OQ-032	Firmware specification
80	Safety mechanisms	SM-04 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. As built nothing observes the motor terminals independently of U7 and the cut-off cannot open (R58 fitted); the IPROPI mirror is blind to a shorted high-side FET (EPB-314). The Q11 reaction ends the apply without releasing it; the credit assumes the stop comes before the force is hazardous (EPB-409, OQ-047) For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052)..	OQ-029	Firmware specification
81	Safety mechanisms	SM-05 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. A correctly framed wrong write is caught only by readback; no CRC on the DRV8263 frame.	OQ-032	Firmware specification
82	Safety mechanisms	SM-06 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The IPROPI current has no sign, so as built the direction is inferred from the profile only For SG-04 the stop keeps the force left when it acts (self-locking spindle); the credit assumes that force plus the other corner's re-clamp holds the vehicle within 1 s (OQ-052)..	OQ-032	Firmware specification
83	Safety mechanisms	SM-07 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The independent source is on another ECU; the rule and the standstill threshold (OQ-035) must be in the technical safety concept.	OQ-038	Firmware specification
84	Safety mechanisms	SM-08 DC	GATED	TI supplies this data on request only. TI claims monitoring of every rail, but the thresholds, deglitch and reaction time sit in the NVM of the fitted variant and the LDO1 monitor shares the die with the regulator; PMC-304 asks whether the core monitor acts before the U14 absolute maximum.	OQ-002	TI data
85	Safety mechanisms	SM-09 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. TI measured about 2 ms from 13.2 V to 12 V off (SDAA375); the path runs through QM transceivers and firmware configuration (OQ-014).	OQ-014	Firmware specification
86	Safety mechanisms	SM-10 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Detects PWM port faults the lockstep cannot see. Reaction STOP only (U5 gates off; release by A-08, PMC-419). As built no threshold, idle-case check or force reference is specified (force is estimated from current and angle, no force sensor): Low. With BLD-108's per-phase check at idle and its HIL test: 0.80, below the Medium ceiling because a fault that makes current look plausible (wrong but commanded pattern) escapes..	OQ-032	Firmware specification
87	Safety mechanisms	SM-11 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. As built nothing removes motor current independently of U5, and nothing frees a motor braked by a shorted phase. With the actions two independent detections (U5 VDS monitor and U14 phase current) feed a reaction outside U5; that argues for the Medium ceiling. Reaction frees the motor, then release is by A-08 (STOP, PMC-419). Driving the isolation from the DRV3263A CUTOFF2 channel, as BLD-201 suggests, would not qualify for U5 die faults..	OQ-023	Firmware specification
88	Safety mechanisms	SM-12 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Single-phase errors break the sum; rail-level readings fail the range check. A common gain error on all three phases passes both and is left to force-versus-position plausibility (BLD-315): Low as built. The second-ADC compare of BLD-315 lifts it, but not to the Medium ceiling while the force reference is itself estimated. Reaction STOP (PMC-419)..	OQ-038	Firmware specification
89	Safety mechanisms	SM-13 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Whether the DRV3263 frame carries a CRC is in the NDA safety manual (OQ-007); readback alone catches a persistent wrong configuration but not a transient one between reads, so below the Medium ceiling. Reaction DRVOFF/nSLEEP, which still works for this mode (STOP, PMC-419)..	OQ-032	Firmware specification

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
90	Safety mechanisms	SM-14 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Credited for single-channel faults only; faults common to both channels are separate rows with their own mechanism (SM-15) or none. As built a sensor in its safe state holds a plausible value on 0.1 uF and is seen only when the rotor moves, and no threshold or debounce is derived (ANG-309): 0.90. With the pull-downs and a derived threshold 0.97, below the High ceiling because slow in-range drift below the threshold is not seen. Reaction STOP (PMC-419)..	OQ-038	Firmware specification
91	Safety mechanisms	SM-15 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Covers LDO1/LDO3 drift inside the PMIC window and ADC faults common to both angle channels. Below the Medium ceiling: a ratiometric error that scales the reference and the sensors together (LDO1 feeds both) is only partly visible. Reaction STOP (PMC-419)..	OQ-038	Firmware specification
92	Safety mechanisms	SM-16 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The profile is not specified, and a request meant for another corner is rejected only if the ECU knows its own position (OQ-040): Medium credited. Reaction REL: U14 and U5 are healthy for these faults, so U14 commands the release and reports the corner unavailable..	OQ-040	Firmware specification
93	Safety mechanisms	SM-20 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Detects gross errors only. It misses deviations below the threshold (ASSUMED; a small offset from U6, the capture path or the clock passes). It also misses low readings during an ABS or ESC intervention, where they look like a locking wheel until the vehicle-reference and wheel-acceleration checks reject them. Timing: speed update 10 ms + CAN cycle 10 ms + 20 ms confirmation = 40 ms, within the 50 ms FTTI above about 10 km/h (48 teeth, 2.0 m, OQ-035). Below that speed the pulse period stretches the detection, but ABS and ESC are assumed inactive there..	OQ-049	Firmware specification
94	Safety mechanisms	SM-21 DC	GATED	TI supplies this data on request only. The MCD detects every absent clock in hardware, and the DCC runs continuously. Errors inside the INTOSC tolerance (about 3 %) are not claimed; they are separate rows (F05-071, F05-072), so the Medium value is kept on the rows it covers. The reaction marks the speed invalid in the next 10 ms frame, within the FTTI. The configuration and its coverage come from the F29P32x safety manual (MCU-204)..	OQ-007	TI data
95	Safety mechanisms	SM-22 DC	UNRELEASED	The device has no public datasheet or safety data. The WSS001 register map, reset flag and frame integrity are unknown, and an internal fault that changes the decoder without changing the register image is not seen, so the value is below the Medium ceiling. Reaction within 20 ms plus one CAN cycle..	OQ-008	TI data
96	Safety mechanisms	SM-23 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. A zero against a moving reference is unambiguous except during an ABS intervention, where it looks like a locked wheel until the lock-time limit, which may exceed the FTTI. ABS intervention is a small fraction of operating time, so the Medium value is argued. Timing: two periods at 10 km/h = 30 ms + CAN 10 ms. Differs from SM-07 (0.99), which rates the standstill decision for SG-03 with no braking dynamics..	OQ-049	Firmware specification
97	Safety mechanisms	SM-24 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Same basis as LM-08. The profile, cycle (10 ms assumed) and timeout (30 ms assumed) are not specified, so the Medium value is credited. A 30 ms timeout is inside the 50 ms FTTI..	OQ-040	Firmware specification
98	Safety mechanisms	SM-30 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The only way the brake controller learns of a corner that loses U14 or both CAN channels (rail, reset or supply faults, PMC-118). A node that has gone silent, or a transmitter that repeats a frozen frame, cannot pass a timeout with an alive counter, so High is argued once the check exists. As built nothing specifies it: no status frame profile, timeout value or reaction (OQ-022, OQ-040), and a U14 that reboots faster than the timeout would come back reporting "available" (PMC-419): Medium, as SM-24. With the actions PMC-118 makes it a vehicle safety requirement proved by HIL fault injection (VCC_6V0 to GND during braking, flagged within 200 ms), and PMC-419's reset-cause rule keeps the corner "unavailable" after an unplanned reset until its start-up tests pass. Timeout monitoring alone is credited at Medium in both scenarios, consistent with SM-24; High would follow from the specified profile and the HIL proof. Timing: 10 ms cycle, 3-frame timeout (30-50 ms) plus redistribution, within the 200 ms provisional FTTI (OQ-021)..	OQ-022	Firmware specification

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
99	Safety mechanisms	SM-31 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Detects a drive that no longer follows its command whatever the cause (U5 outputs off, lost gate supply, open FET, phase or shunt, PWM or disable pin stuck), which is silent otherwise because the corner keeps reporting "available". As built the DFMEA only asks for it (BLD-104, BLD-110, BLD-202): no threshold, time or reaction: Low. With BLD-104's 50 ms threshold, BLD-110/BLD-202's per-phase check and their fault-injection tests, the Medium ceiling is argued: a lost or open phase is a gross, unambiguous discrepancy between command and current. Not claimed: a slow build-up that stays within current limits (FE-06), which needs the response budget of BLD-225 (OQ-021). Reaction RPT: U14 is healthy for every mode it is credited on..	OQ-032	Firmware specification
100	Safety mechanisms	SM-32 DC	GATED	TI supplies this data on request only. Detection alone does not reach the SG-02 safe state: the reset silences the corner and the brake controller learns of it only by SM-30. Coverage taken as the product of the two, SM-01 × SM-30: 0.99 × 0.90 as built, 0.99 × 0.99 with the actions..	OQ-007	TI data
101	Safety mechanisms	SM-33 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Product SM-02 × SM-30: 0.90 × 0.90 in both scenarios (SM-30 is Medium in both). A U14 that stops its status frames is seen by the timeout even if the watchdog misses it, so the product is conservative..	OQ-002	TI data
102	Safety mechanisms	SM-34 DC	GATED	TI supplies this data on request only. Product SM-08 × SM-30: 0.90 × 0.90 in both scenarios (SM-30 is Medium in both). The LDO1 undervoltage threshold must sit above 2.65 V or both angle channels freeze before the reset (ANG-305, OQ-002)..	OQ-002	TI data
103	Safety mechanisms	SM-40 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Credited where the EPB drive path itself cannot be used for the reaction (U14 EPB pins stuck): the report does not need the stuck pins. As built there is no threshold or debounce, the IPROPI mirror is blind to current that does not pass a gate-driven high-side FET (EPB-314), nothing stops the release, so this corner loses all its force and the hold rests on the other corner alone: Low. With the actions the terminal readback gives a second observation and Q11/SAFE_OUT1 stop the release, so the spindle keeps what is left: the Medium ceiling is argued on two independent observations and a reaction outside the failed part. Not High: the other corner's re-clamp and its timing within the 1 s FTTI are not specified (new question on single-corner hold)..	OQ-032	Firmware specification
104	Safety mechanisms	SM-41 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Covers faults that leave the EPB unable to drive (U7 outputs off, Q11 or its drive open, pads open, U7 asleep or held off). A held EPB keeps its force when these faults occur (self-locking, OQ-023); they matter at the next apply, where the absence of current or of a stall is unambiguous. The check runs on every apply and reports before the driver leaves the vehicle, and its reaction does not use the failed part, so the Medium ceiling is argued. Not High: the hold after the report relies on the other corner and the park lock (vehicle level), and a fault that lets current flow but weakens the force is left to SM-42. Same value in both scenarios: the check uses the as-built current sense..	OQ-032	Firmware specification
105	Safety mechanisms	SM-42 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Catches a reading stuck high or offset (rest check) and an apply that stalls too early (run time), but not a gain error inside the plausibility window: there is no second measurement of EPB current or force (EPB-309, EPB-318). The actions add no second measurement, so Low in both scenarios. A current reading that is too high is safe-side for SG-03 (an early stop) and the hazard for SG-04 (an early false stall)..	OQ-043	Firmware specification
106	Safety mechanisms	SM-43 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Same basis as SM-16 and LM-08: the profile and data ID are not specified, so Medium is credited. The reaction differs from SM-16 (release to zero force): for a parking or standstill-hold request a failed check keeps the hold, which needs no working actuator..	OQ-040	Firmware specification
107	Safety mechanisms	SM-70 DC	JUDGMENT	Value set by sev10 engineering judgment. Credited only on the rows defined as hard (above the breaker band) downstream of R7, so the resistive faults it cannot see are not in its coverage. Kept below the High ceiling because a crack or bridge that sputters (intermittent contact, carbon path forming and burning off) can drop below 18 A before the 1 ms timer ends and restart it, and the thresholds carry the R7, R11 and IMON-free tolerance of the set network (SUP-314); nothing tests the comparators (their loss is latent, F07-020, F07-021, F07-026). Acts in microseconds to a millisecond, far inside any time to ignition. The 1.4-1.6 J the bulk dumps into the fault first is not a sustained source..	OQ-028	Client data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
108	Safety mechanisms	SM-71 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. IMON resolves about 3 A (offset +/-2.1 mV = +/-2.1 A at 1 mOhm, gain +/-12.5 %), about 160 W at 54 V, so resistive faults of 2-3 A and the low-power start of a crack or CAF path are missed (PCB-202). The Low ceiling is argued because the covered high-power end is the part that ignites fastest, and a carbonising path tends to fall in resistance into the covered band before it ignites. It runs only downstream of R7 and only with the bridges idle for the idle check; the drive-time balance is not credited. Check period and debounce must sit inside the time to ignition at about 1 kW, which is unknown (OQ-044). Reaction depends on INH, U1 EN and Q1 (tested by LM-13); IMON itself by LM-70..	OQ-044	Firmware specification
109	Safety mechanisms	SM-72 DC	GATED	TI supplies this data on request only. Credited only on the 12 V rows defined as hard (below the hiccup entry). The limit and hiccup entry level are not characterised against a partly resistive short, and U2's FMEDA is on request (OQ-007): Medium. A loss of the limit is latent with no test (F07-063)..	OQ-007	TI data
110	Safety mechanisms	SM-73 DC	NO-CLIENT-DATA	Mission-profile value not supplied; SN 29500-order value used. The only limit ahead of R7. Rating and clearing time are not specified (OQ-025): a short between the corner's peak draw and the fuse's fast-clear current heats the input copper, J3/J4, L1 and Q1 for seconds or more, and a fuse shared by several corners is sized above one corner's short. The Low ceiling is argued only because the rows credited are metallic shorts ahead of R7 (TVS junction, pad bridge, hard capacitor short), which draw the battery's short-circuit current far above any feed-fuse rating; the SUP-220 action (dedicated, sized fuse) is what would justify more..	OQ-025	Client data
111	Safety mechanisms	LM-01 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Tests the pin, the pull-up and the U7 input once per operation.	OQ-032	Firmware specification
112	Safety mechanisms	LM-02 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. A blind sense path shows no inrush at the next commanded operation.	OQ-032	Firmware specification
113	Safety mechanisms	LM-03 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. As built the cut-off is defeated by R58, so no test can show it works; with R58 not fitted the test covers Q11, R87, Q6 and CUTOFF1.	OQ-029	Firmware specification
114	Safety mechanisms	LM-04 DC	GATED	TI supplies this data on request only. TI's safety manual defines the tests and their coverage; not public.	OQ-007	TI data
115	Safety mechanisms	LM-05 DC	GATED	TI supplies this data on request only. TI's PMIC safety manual defines the BIST coverage; the reset-path test is a software requirement.	OQ-007	TI data
116	Safety mechanisms	LM-06 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. A dead or corrupted readback fails the fixed status bits on the next access.	OQ-032	Firmware specification
117	Safety mechanisms	LM-07 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Detects OUTx shorts to VM or GND at rest; not every harness short.	OQ-032	Firmware specification
118	Safety mechanisms	LM-08 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The profile and data ID of the speed message are not specified yet; credited at Medium until they are.	OQ-038	Firmware specification
119	Safety mechanisms	LM-10 DC	GATED	TI supplies this data on request only. Coverage of the VDS and Rsense comparators and of nFAULT by ABIST is not published (OQ-007); credited Low.	OQ-007	TI data
120	Safety mechanisms	LM-11 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The test exercises the whole path (U14 pin, net, U5 input, gate outputs) and checks the result by phase current, so the Medium ceiling is argued; it runs once per drive enable.	OQ-032	Firmware specification
121	Safety mechanisms	LM-12 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Same detection and same limits as SM-14, applied to the channel that is not used for commutation.	OQ-038	Firmware specification
122	Safety mechanisms	LM-13 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Tests U1, Q1 and both INH paths once per drive cycle; does not test the VMON divider scale, and the cut-off is not latched (OQ-041).	OQ-014	Firmware specification
123	Safety mechanisms	LM-14 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. The force-travel relation depends on the pedal feel simulator and catches only large errors; an open wire reads just above the valid band (PED-104, PED-302).	OQ-009	Firmware specification
124	Safety mechanisms	LM-15 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Tests each switch of the isolation individually by its effect on current, so the Medium ceiling is argued.	OQ-032	Firmware specification
125	Safety mechanisms	LM-20 DC	UNRELEASED	The device has no public datasheet or safety data. A dead or stuck SDO is seen only if the WSS001 frame has fixed bits or a CRC, which is unknown (OQ-008), and the SDOEPB idle level is undefined on VerB (WSS-314). Low until the frame format is known..	OQ-008	TI data
126	Safety mechanisms	LM-40 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Detects a corrupted or missing status from this corner, which would otherwise hide a hold loss from the other corner and the driver. The profile and timeout are not specified, so Medium is credited, as for SM-24. The DFMEA has no row for the EPB status path; EPB-510 and EPB-505 only require the report..	OQ-040	Firmware specification

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
127	Safety mechanisms	LM-70 DC	PROVISIONAL	Software mechanism specified in the DFMEA, not yet implemented or verified. Same argument as LM-02: a stuck or scaled IMON fails the next actuation, which gives a stimulus of several amps. Medium ceiling argued because every drive cycle actuates the brake many times..	OQ-032	Firmware specification
128	SG-01	FTTI	NO-CLIENT-DATA	TBD; provisional 100 ms (ASSUMED). Fault-tolerant time interval for SG-01; the technical safety concept sets it.	OQ-021	Client data
129	SG-02	FTTI	NO-CLIENT-DATA	TBD; provisional 200 ms (ASSUMED). Fault-tolerant time interval for SG-02; the technical safety concept sets it.	OQ-021	Client data
130	SG-03	FTTI	NO-CLIENT-DATA	TBD; provisional 300 ms (ASSUMED). Fault-tolerant time interval for SG-03; the technical safety concept sets it.	OQ-021	Client data
131	SG-04	FTTI	NO-CLIENT-DATA	TBD; provisional 1 s (ASSUMED). Fault-tolerant time interval for SG-04; the technical safety concept sets it.	OQ-021	Client data
132	SG-05	FTTI	NO-CLIENT-DATA	TBD; provisional 50 ms (ASSUMED). Fault-tolerant time interval for SG-05; the technical safety concept sets it.	OQ-021	Client data
133	SG-07	FTTI	NO-CLIENT-DATA	TBD; U1 acts in microseconds to 1 ms, the IMON check needs the time to ignition to exceed its period plus debounce (ASSUMED, OQ-044). Fault-tolerant time interval for SG-07; the technical safety concept sets it.	OQ-021	Client data
134	SG-01	F01-001 share	JUDGMENT	Failure-mode share of U5 set by sev10: Input logic or state-machine fault drives the inverter regardless of DRVOFF, nSLEEP and PWM inputs	OQ-007	TI data
135	SG-01	F01-002 share	JUDGMENT	Failure-mode share of U5 set by sev10: One gate-drive output stage stuck on (source stuck, sink lost): FET held on whatever U5 is commanded	OQ-007	TI data
136	SG-01	F01-003 share	JUDGMENT	Failure-mode share of U5 set by sev10: DRVOFF or nSLEEP input no longer disables the gate drivers	OQ-007	TI data
137	SG-01	F01-004 share	JUDGMENT	Failure-mode share of U5 set by sev10: Current-sense amplifier gain, offset or output wrong (one phase or all three), or VREF input fault	OQ-007	TI data
138	SG-01	F01-005 share	JUDGMENT	Failure-mode share of U5 set by sev10: Register corruption changes the drive configuration (PWM mode, dead time, CSA gain, protection) without a valid write	OQ-007	TI data
139	SG-01	F01-006 share	JUDGMENT	Failure-mode share of U5 set by sev10: VDS or Rsense overcurrent comparators, or their nFAULT report, lost or wrong	OQ-007	TI data
140	SG-01	F01-007 share	JUDGMENT	Failure-mode share of U5 set by sev10: Outputs off or high impedance, GVDD, charge pump or internal supply fault, thermal shutdown and other faults that stop the drive	OQ-007	TI data
141	SG-01	F01-008 share	JUDGMENT	Failure-mode share of U5 set by sev10: CUTOFF1 and CUTOFF2 channels	OQ-007	TI data
142	SG-01	F01-009 share	JUDGMENT	Failure-mode share of U5 support passives set by sev10: Open, short or drift of GVDD, charge-pump and bootstrap parts, SPI series resistors and the nFAULT pull-up	OQ-007	TI data
143	SG-01	F01-026 share	JUDGMENT	Failure-mode share of Bus capacitors set by sev10: Short, open, capacitance loss or ESR rise on 48V/12V_P	OQ-007	TI data
144	SG-01	F01-032 share	JUDGMENT	Failure-mode share of CSA front end set by sev10: Open, short or drift of a Kelvin, filter or SOx part: one phase reads 0 A, offset, frozen or noisy	OQ-007	TI data
145	SG-01	F01-033 share	JUDGMENT	Failure-mode share of CSA front end set by sev10: Faults without a reading error (filter capacitance loss within the error budget, drift within tolerance)	OQ-007	TI data
146	SG-01	F01-036 share	JUDGMENT	Failure-mode share of ADC reference network set by sev10: Ferrite open or capacitor short: VREFHI or VDDA of one ADC group lost	OQ-007	TI data
147	SG-01	F01-037 share	JUDGMENT	Failure-mode share of ADC reference network set by sev10: Capacitor open or capacitance loss, ferrite degraded	OQ-007	TI data
148	SG-01	F01-040 share	JUDGMENT	Failure-mode share of U12 set by sev10: SIN/COS in range but wrong (offset, gain, phase) or quadrant outputs wrong	OQ-007	TI data
149	SG-01	F01-041 share	JUDGMENT	Failure-mode share of U12 set by sev10: Output stuck at a rail or out of the 10-90 % band	OQ-007	TI data
150	SG-01	F01-042 share	JUDGMENT	Failure-mode share of U12 set by sev10: Internal diagnostic puts U12 in its safe state: outputs Hi-Z and held in range on C110/C111	OQ-007	TI data
151	SG-01	F01-043 share	JUDGMENT	Failure-mode share of U12 set by sev10: Faults without an output error (supply current, internal redundancy)	OQ-007	TI data
152	SG-01	F01-044 share	JUDGMENT	Failure-mode share of U13 set by sev10: Output wrong in range, stuck, frozen (Hi-Z) or quadrant wrong	OQ-007	TI data
153	SG-01	F01-045 share	JUDGMENT	Failure-mode share of U13 set by sev10: Faults without an output error	OQ-007	TI data
154	SG-01	F01-050 share	JUDGMENT	Failure-mode share of Angle front end ch1 set by sev10: Open, short or drift on SIN_P1/COS_P1, Q01/Q11 or the U12 supply pin	OQ-007	TI data
155	SG-01	F01-051 share	JUDGMENT	Failure-mode share of Angle front end ch1 set by sev10: Faults within the error budget (decoupling open, small drift)	OQ-007	TI data
156	SG-01	F01-052 share	JUDGMENT	Failure-mode share of Angle front end ch2 set by sev10: Open, short or drift on SIN_P2/COS_P2, Q02/Q12 or the U13 supply pin	OQ-007	TI data
157	SG-01	F01-053 share	JUDGMENT	Failure-mode share of Angle front end ch2 set by sev10: Faults within the error budget	OQ-007	TI data
158	SG-01	F01-060 share	JUDGMENT	Failure-mode share of U14 set by sev10: CPU, memory or bus fault produces a wrong torque or force command	OQ-007	TI data

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159	SG-01	F01-061 share	JUDGMENT	Failure-mode share of U14 set by sev10: Fault common to both lockstep cores (internal clock, core supply, reset logic) that upsets program flow	OQ-007	TI data
160	SG-01	F01-062 share	JUDGMENT	Failure-mode share of U14 set by sev10: BLDC PWM output pins (U14.88-93) stuck or shorted (port fault the lockstep does not see)	OQ-007	TI data
161	SG-01	F01-063 share	JUDGMENT	Failure-mode share of U14 set by sev10: DRVOFF (U14.87) or nSLEEP (U14.86) pin stuck in the enable state	OQ-007	TI data
162	SG-01	F01-064 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC channel, multiplexer or sample-and-hold fault on a phase-current input	OQ-007	TI data
163	SG-01	F01-065 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC channel fault on one angle input	OQ-007	TI data
164	SG-01	F01-066 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC module or reference fault common to both angle channels (both converted on one module)	OQ-007	TI data
165	SG-01	F01-067 share	JUDGMENT	Failure-mode share of U14 set by sev10: MCAN peripheral or message-RAM fault delivers a wrong, stale or misaddressed clamp-force request	OQ-007	TI data
166	SG-01	F01-068 share	JUDGMENT	Failure-mode share of U14 set by sev10: Lockstep comparator, ECC or error-signal module fault	OQ-007	TI data
167	SG-01	F01-069 share	JUDGMENT	Failure-mode share of U14 set by sev10: Other MCU functions (EPB, wheel speed, pedal SENT capture, other peripherals)	OQ-007	TI data
168	SG-01	F01-070 share	JUDGMENT	Failure-mode share of U3 set by sev10: Watchdog or error monitor fails to act, or NRST cannot reset the MCU	OQ-007	TI data
169	SG-01	F01-071 share	JUDGMENT	Failure-mode share of U3 set by sev10: SAFE_OUT1 fails to assert in the safe state	OQ-007	TI data
170	SG-01	F01-072 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 (3.3 V: U14 I/O, U5 logic, U12/U13) or LDO3 (3.3Vref) regulates outside its monitor window, high or low	OQ-007	TI data
171	SG-01	F01-073 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 or LDO3 drifts inside the monitor window	OQ-007	TI data
172	SG-01	F01-074 share	JUDGMENT	Failure-mode share of U3 set by sev10: Rail monitors (EXT_VMON1, LDO1, LDO3) stuck at 'good'	OQ-007	TI data
173	SG-01	F01-075 share	JUDGMENT	Failure-mode share of U3 set by sev10: Spurious reset or safe state	OQ-007	TI data
174	SG-01	F01-076 share	JUDGMENT	Failure-mode share of U3 set by sev10: Other PMIC functions (buck-boost, LDO2, PLDO1/2 pedal supplies, EPB-related, rails lost)	OQ-007	TI data
175	SG-01	F01-080 share	JUDGMENT	Failure-mode share of U4 set by sev10: 1.25 V core regulated high (half of TI's 'output out of specification' mode)	OQ-007	TI data
176	SG-01	F01-081 share	JUDGMENT	Failure-mode share of U4 set by sev10: High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	OQ-007	TI data
177	SG-01	F01-083 share	JUDGMENT	Failure-mode share of R46, R48 set by sev10: R46 open or R48 short: feedback at 0 V, U4 drives the core high	OQ-007	TI data
178	SG-01	F01-084 share	JUDGMENT	Failure-mode share of R46, R48 set by sev10: R46 short, R48 open, drift within tolerance	OQ-007	TI data
179	SG-01	F01-100 share	JUDGMENT	Failure-mode share of U2 set by sev10: High-side FET short: 12 V rail pulled toward 48V/12V_P	OQ-007	TI data
180	SG-01	F01-101 share	JUDGMENT	Failure-mode share of U2 set by sev10: Output low or lost, regulation faults within the PMIC input range	OQ-007	TI data
181	SG-01	F01-102 share	JUDGMENT	Failure-mode share of R33, R35 set by sev10: R33 open or R35 short: feedback at 0 V, U2 drives 12 V toward the input	OQ-007	TI data
182	SG-01	F01-103 share	JUDGMENT	Failure-mode share of R33, R35 set by sev10: R33 short, R35 open, drift within tolerance	OQ-007	TI data
183	SG-01	F01-113 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 drain-source short (40 % of Q1)	OQ-007	TI data
184	SG-01	F01-114 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 other modes; any Q2 mode (reverse blocking)	OQ-007	TI data
185	SG-01	F01-115 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Transceiver stays awake when nSTB_CAN goes low (INH held high)	OQ-007	TI data
186	SG-01	F01-116 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	OQ-007	TI data
187	SG-01	F01-117 share	JUDGMENT	Failure-mode share of INH network set by sev10: R156 open: INH_CAN floats instead of going low	OQ-007	TI data
188	SG-01	F01-118 share	JUDGMENT	Failure-mode share of INH network set by sev10: Other faults (diode open or short, series resistors)	OQ-007	TI data
189	SG-01	F01-140 share	JUDGMENT	Failure-mode share of Pedal input networks set by sev10: Open, short or drift: pedal value offset, scaled, stuck or following another channel	OQ-007	TI data
190	SG-01	F01-141 share	JUDGMENT	Failure-mode share of Pedal input networks set by sev10: Faults without a value error (filter capacitance loss, drift within the SENT timing budget)	OQ-007	TI data
191	SG-01	F01-150 share	JUDGMENT	Failure-mode share of New (BLD-102) set by sev10: Open of the DRVOFF pull-up or the nSLEEP pull-down: U5 not held off while U14 is in reset	OQ-007	TI data
192	SG-01	F01-151 share	JUDGMENT	Failure-mode share of New (BLD-102) set by sev10: Other modes (PWM or nCS pulls, shorts, drift)	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
193	SG-02	F02-001 share	JUDGMENT	Failure-mode share of U5 set by sev10: Input logic or state-machine fault drives the inverter regardless of DRVOFF, nSLEEP and PWM inputs	OQ-007	TI data
194	SG-02	F02-002 share	JUDGMENT	Failure-mode share of U5 set by sev10: One gate-drive output stage stuck on (source stuck, sink lost)	OQ-007	TI data
195	SG-02	F02-003 share	JUDGMENT	Failure-mode share of U5 set by sev10: Current-sense amplifier gain, offset or output wrong (one phase or all three), or VREF input fault	OQ-007	TI data
196	SG-02	F02-004 share	JUDGMENT	Failure-mode share of U5 set by sev10: Register corruption changes the drive configuration (PWM mode, dead time, CSA gain, protection thresholds) without a valid write	OQ-007	TI data
197	SG-02	F02-005 share	JUDGMENT	Failure-mode share of U5 set by sev10: Outputs off or high impedance, GVDD, charge-pump, bootstrap or internal-supply fault, thermal shutdown, spurious VDS/Rsense trip or false nFAULT	OQ-007	TI data
198	SG-02	F02-006 share	JUDGMENT	Failure-mode share of U5 set by sev10: DRVOFF or nSLEEP no longer disables; VDS/Rsense protection lost; CUTOFF1 and CUTOFF2 channels	OQ-007	TI data
199	SG-02	F02-007 share	JUDGMENT	Failure-mode share of U5 support passives set by sev10: GVDD, VCP or bootstrap capacitor short or open, bootstrap resistor open, DVDD or SPI series resistor open	OQ-007	TI data
200	SG-02	F02-008 share	JUDGMENT	Failure-mode share of U5 support passives set by sev10: Capacitance loss or drift within the TI requirement; nFAULT pull-up faults	OQ-007	TI data
201	SG-02	F02-025 share	JUDGMENT	Failure-mode share of Bus capacitors set by sev10: Short (hard or resistive) on 48V/12V_P	OQ-007	TI data
202	SG-02	F02-026 share	JUDGMENT	Failure-mode share of Bus capacitors set by sev10: Open, capacitance loss or ESR rise	OQ-007	TI data
203	SG-02	F02-032 share	JUDGMENT	Failure-mode share of CSA front end set by sev10: Open, short or drift of a Kelvin, filter or SOx part: one phase reads high, offset, frozen or noisy	OQ-007	TI data
204	SG-02	F02-033 share	JUDGMENT	Failure-mode share of CSA front end set by sev10: Faults without a reading error	OQ-007	TI data
205	SG-02	F02-036 share	JUDGMENT	Failure-mode share of ADC reference network set by sev10: Ferrite open or capacitor short: VREFHI or VDDA of one ADC group lost	OQ-007	TI data
206	SG-02	F02-037 share	JUDGMENT	Failure-mode share of ADC reference network set by sev10: Capacitor open or capacitance loss, ferrite degraded	OQ-007	TI data
207	SG-02	F02-040 share	JUDGMENT	Failure-mode share of U12 set by sev10: SIN/COS wrong in range (offset, gain, phase), quadrant outputs wrong, or output stuck at a rail	OQ-007	TI data
208	SG-02	F02-041 share	JUDGMENT	Failure-mode share of U12 set by sev10: Internal diagnostic puts U12 in its safe state: outputs Hi-Z and held in range on C110/C111	OQ-007	TI data
209	SG-02	F02-042 share	JUDGMENT	Failure-mode share of U12 set by sev10: Faults without an output error	OQ-007	TI data
210	SG-02	F02-043 share	JUDGMENT	Failure-mode share of U13 set by sev10: Output wrong in range, stuck, frozen (Hi-Z) or quadrant wrong	OQ-007	TI data
211	SG-02	F02-044 share	JUDGMENT	Failure-mode share of U13 set by sev10: Faults without an output error	OQ-007	TI data
212	SG-02	F02-050 share	JUDGMENT	Failure-mode share of Angle front end ch1 set by sev10: Open, short or drift on SIN_P1/COS_P1, Q01/Q11 or the U12 supply pin	OQ-007	TI data
213	SG-02	F02-051 share	JUDGMENT	Failure-mode share of Angle front end ch1 set by sev10: Faults within the error budget	OQ-007	TI data
214	SG-02	F02-052 share	JUDGMENT	Failure-mode share of Angle front end ch2 set by sev10: Open, short or drift on SIN_P2/COS_P2, Q02/Q12 or the U13 supply pin	OQ-007	TI data
215	SG-02	F02-053 share	JUDGMENT	Failure-mode share of Angle front end ch2 set by sev10: Faults within the error budget	OQ-007	TI data
216	SG-02	F02-060 share	JUDGMENT	Failure-mode share of U14 set by sev10: CPU, memory or bus fault produces a wrong, low or frozen torque command	OQ-007	TI data
217	SG-02	F02-061 share	JUDGMENT	Failure-mode share of U14 set by sev10: Fault common to both lockstep cores (internal clock, core supply, reset logic) that upsets program flow	OQ-007	TI data
218	SG-02	F02-062 share	JUDGMENT	Failure-mode share of U14 set by sev10: BLDC PWM output pins (U14.88-93) stuck or shorted, or DRVOFF (U14.87) or nSLEEP (U14.86) stuck in the disable state	OQ-007	TI data
219	SG-02	F02-063 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC channel, multiplexer or sample-and-hold fault on a phase-current input	OQ-007	TI data
220	SG-02	F02-064 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC channel fault on one angle input	OQ-007	TI data
221	SG-02	F02-065 share	JUDGMENT	Failure-mode share of U14 set by sev10: ADC module or reference fault common to both angle channels (both converted on one module)	OQ-007	TI data
222	SG-02	F02-066 share	JUDGMENT	Failure-mode share of U14 set by sev10: MCAN peripheral or message-RAM fault delivers a wrong, stale or lost clamp-force request	OQ-007	TI data
223	SG-02	F02-067 share	JUDGMENT	Failure-mode share of U14 set by sev10: Status transmit path (MCAN TX, message RAM) or flash/boot fault: status frames lost, frozen, or U14 does not start	OQ-007	TI data
224	SG-02	F02-068 share	JUDGMENT	Failure-mode share of U14 set by sev10: SPI peripheral to U5 writes wrong data or corrupts readback	OQ-007	TI data
225	SG-02	F02-069 share	JUDGMENT	Failure-mode share of U14 set by sev10: Lockstep comparator, ECC or error-signal module fault	OQ-007	TI data
226	SG-02	F02-070 share	JUDGMENT	Failure-mode share of U14 set by sev10: Other MCU functions (EPB, wheel speed, pedal capture, other peripherals); DRVOFF or nSLEEP pin stuck in the enable state	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
227	SG-02	F02-080 share	JUDGMENT	Failure-mode share of U3 set by sev10: Watchdog or error monitor fails to act, or NRST cannot reset the MCU	OQ-007	TI data
228	SG-02	F02-081 share	JUDGMENT	Failure-mode share of U3 set by sev10: SAFE_OUT1 asserts without a fault	OQ-007	TI data
229	SG-02	F02-082 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 (3.3 V), LDO3 (3.3Vref), LDO2 (5 V) or the buck-boost regulates outside its monitor window, high or low	OQ-007	TI data
230	SG-02	F02-083 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 or LDO3 drifts inside the monitor window	OQ-007	TI data
231	SG-02	F02-084 share	JUDGMENT	Failure-mode share of U3 set by sev10: Rail monitors (EXT_VMON1, LDO1, LDO2, LDO3, BB_OUT) stuck at 'good'	OQ-007	TI data
232	SG-02	F02-085 share	JUDGMENT	Failure-mode share of U3 set by sev10: Spurious reset or safe state (NRST asserted, U14 held in reset or cycling)	OQ-007	TI data
233	SG-02	F02-086 share	JUDGMENT	Failure-mode share of U3 set by sev10: Buck-boost (VCC_6V0) lost; LDO1, LDO2 or LDO3 output lost (current limit, thermal or internal-supply shutdown); SPI or internal supply lost	OQ-007	TI data
234	SG-02	F02-092 share	JUDGMENT	Failure-mode share of U3 set by sev10: Other PMIC functions (PLDO1/2 pedal supplies, EPB-related, LDO4, LDO2 low in a band where only U6 is affected); SAFE_OUT1 fails to assert	OQ-007	TI data
235	SG-02	F02-100 share	JUDGMENT	Failure-mode share of U4 set by sev10: 1.25 V core regulated high or low (TI 'output out of specification'), or high-side FET stuck on	OQ-007	TI data
236	SG-02	F02-120 share	JUDGMENT	Failure-mode share of U2 set by sev10: Output lost or below the CMPSS undervoltage level; high-side FET short (12 V pulled toward 48V/12V_P)	OQ-007	TI data
237	SG-02	F02-121 share	JUDGMENT	Failure-mode share of U2 set by sev10: 12 V output low in a band where U3 and U14 run but U5 GVDD is below its requirement	OQ-007	TI data
238	SG-02	F02-131 share	JUDGMENT	Failure-mode share of U1 set by sev10: HGATE out of spec or stuck low (TI 26 %); false OCP, SCP, UV or OV trip; pin short that switches Q1 off	OQ-007	TI data
239	SG-02	F02-132 share	JUDGMENT	Failure-mode share of U1 set by sev10: DGATE modes (TI 40 %), HGATE stuck high (5 %), lost OCP/SCP/UV/OV protection	OQ-007	TI data
240	SG-02	F02-133 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 drain-source open or gate-source short; Q2 drain-source open	OQ-007	TI data
241	SG-02	F02-134 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 short or on-resistance increase; Q2 short, gate-source short or on-resistance increase	OQ-007	TI data
242	SG-02	F02-135 share	JUDGMENT	Failure-mode share of INH network set by sev10: INH_CAN pulled or held low (diode open in the only active path, series resistor open, node shorted to GND)	OQ-007	TI data
243	SG-02	F02-136 share	JUDGMENT	Failure-mode share of INH network set by sev10: One transceiver's INH contribution lost (the other holds INH_CAN); R156 open	OQ-007	TI data
244	SG-02	F02-138 share	JUDGMENT	Failure-mode share of Supply passives set by sev10: Series part open (inductor, shunt, link, Q3), shunt drifting high, capacitor or TVS short, VSUP dropper open, U1/U2 divider fault that trips or disables the supply	OQ-007	TI data
245	SG-02	F02-139 share	JUDGMENT	Failure-mode share of Supply passives set by sev10: Capacitor open or capacitance loss, TVS open, shunt drifting low, Q3 short, divider drift inside its window	OQ-007	TI data
246	SG-02	F02-160 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Receiver or transmitter fail, stuck in sleep, bus dominant (TI 35 + 35 + 15 + 5 %)	OQ-007	TI data
247	SG-02	F02-161 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Pin-to-pin short (TI 5 %): VCC, VIO or INH shorted	OQ-007	TI data
248	SG-02	F02-170 share	JUDGMENT	Failure-mode share of New (BLD-102, BLD-120) set by sev10: Pull resistor short (holds DRVOFF high, nSLEEP, a PWM input or nCS at the off level), or the nSLEEP series resistor open	OQ-007	TI data
249	SG-02	F02-171 share	JUDGMENT	Failure-mode share of New (BLD-102, BLD-120) set by sev10: Pull resistor open or drift; series resistor short or drift	OQ-007	TI data
250	SG-03	F03-001 share	JUDGMENT	Failure-mode share of U7 set by sev10: Output stage drives the motor in the apply direction without a command (diagonal FET pair shorted or gate drive stuck on)	OQ-007	TI data
251	SG-03	F03-002 share	JUDGMENT	Failure-mode share of U7 set by sev10: Output stage drives the release direction without a command	OQ-007	TI data
252	SG-03	F03-003 share	JUDGMENT	Failure-mode share of U7 set by sev10: Input logic fault (EN/IN1 or PH/IN2 buffer, state machine) drives the bridge without a command	OQ-007	TI data
253	SG-03	F03-004 share	JUDGMENT	Failure-mode share of U7 set by sev10: DRVOFF no longer disables the bridge	OQ-007	TI data
254	SG-03	F03-005 share	JUDGMENT	Failure-mode share of U7 set by sev10: Current-sense output (IPROPI) wrong or zero	OQ-007	TI data
255	SG-03	F03-006 share	JUDGMENT	Failure-mode share of U7 set by sev10: Register corruption unlocks SPI control and commands a drive (S_DRVOFF = 0, S_ENIN1 = 1)	OQ-007	TI data
256	SG-03	F03-007 share	JUDGMENT	Failure-mode share of U7 set by sev10: Fault reporting (nFAULT, STATUS, SPI readback) lost or wrong	OQ-007	TI data
257	SG-03	F03-008 share	JUDGMENT	Failure-mode share of U7 set by sev10: Outputs off or high impedance; the bridge cannot drive	OQ-007	TI data
258	SG-03	F03-009 share	JUDGMENT	Failure-mode share of U7 set by sev10: VM or GND pin short, internal supply short	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
259	SG-03	F03-012 share	JUDGMENT	Failure-mode share of U7 set by sev10: OUTA or OUTB pin shorted to VM or GND	OQ-007	TI data
260	SG-03	F03-010 share	JUDGMENT	Failure-mode share of U7 set by sev10: Over-current protection lost	OQ-007	TI data
261	SG-03	F03-013 share	JUDGMENT	Failure-mode share of U7 set by sev10: Thermal protection lost	OQ-007	TI data
262	SG-03	F03-011 share	JUDGMENT	Failure-mode share of U7 set by sev10: Other internal faults (charge pump, oscillator, SPI timing) that stop the bridge	OQ-007	TI data
263	SG-03	F03-020 share	JUDGMENT	Failure-mode share of U14 set by sev10: CPU, memory or bus fault produces an erroneous EPB apply command	OQ-007	TI data
264	SG-03	F03-021 share	JUDGMENT	Failure-mode share of U14 set by sev10: EPB control pins (U14.2 DRVOFF, U14.11, U14.98) stuck in the drive state (port fault the lockstep does not see)	OQ-007	TI data
265	SG-03	F03-022 share	JUDGMENT	Failure-mode share of U14 set by sev10: SPI-D peripheral fault writes wrong data to U7	OQ-007	TI data
266	SG-03	F03-023 share	JUDGMENT	Failure-mode share of U14 set by sev10: Lockstep comparator, ECC or error-signal module fault	OQ-007	TI data
267	SG-03	F03-024 share	JUDGMENT	Failure-mode share of U14 set by sev10: Isense_EPB ADC channel reads wrong	OQ-007	TI data
268	SG-03	F03-026 share	JUDGMENT	Failure-mode share of U14 set by sev10: CAN receive path (MCAN, message RAM) delivers a wrong vehicle speed	OQ-007	TI data
269	SG-03	F03-025 share	JUDGMENT	Failure-mode share of U14 set by sev10: Other MCU functions (BLDC control, other peripherals)	OQ-007	TI data
270	SG-03	F03-030 share	JUDGMENT	Failure-mode share of U3 set by sev10: Watchdog or error monitor fails to act, or NRST cannot reset the MCU	OQ-007	TI data
271	SG-03	F03-031 share	JUDGMENT	Failure-mode share of U3 set by sev10: SAFE_OUT1 fails to assert in the safe state	OQ-007	TI data
272	SG-03	F03-034 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 (3.3 V, MCU I/O and U7 logic) regulates high	OQ-007	TI data
273	SG-03	F03-035 share	JUDGMENT	Failure-mode share of U3 set by sev10: Rail monitors (EXT_VMON1 on the 1.25 V core, LDO overvoltage) stuck at 'good'	OQ-007	TI data
274	SG-03	F03-032 share	JUDGMENT	Failure-mode share of U3 set by sev10: Spurious reset or safe state	OQ-007	TI data
275	SG-03	F03-033 share	JUDGMENT	Failure-mode share of U3 set by sev10: Other PMIC functions (regulators low or lost, pedal supplies, other monitors)	OQ-007	TI data
276	SG-03	F03-110 share	JUDGMENT	Failure-mode share of U4 set by sev10: 1.25 V core regulated high (half of TI's 'output out of specification' mode)	OQ-007	TI data
277	SG-03	F03-111 share	JUDGMENT	Failure-mode share of U4 set by sev10: High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	OQ-007	TI data
278	SG-03	F03-120 share	JUDGMENT	Failure-mode share of U2 set by sev10: High-side FET short: 12 V rail pulled toward 48V/12V_P	OQ-007	TI data
279	SG-03	F03-121 share	JUDGMENT	Failure-mode share of U2 set by sev10: Output low or lost, regulation faults within the PMIC input range	OQ-007	TI data
280	SG-03	F03-040 share	JUDGMENT	Failure-mode share of U5 set by sev10: CUTOFF1 output stuck on	OQ-007	TI data
281	SG-03	F03-041 share	JUDGMENT	Failure-mode share of U5 set by sev10: CUTOFF1 output stuck off	OQ-007	TI data
282	SG-03	F03-042 share	JUDGMENT	Failure-mode share of U5 set by sev10: Other gate-driver functions (BLDC bridge)	OQ-007	TI data
283	SG-03	F03-100 share	UNRELEASED	Failure-mode share of U6 set by sev10: Standstill reported while the wheel turns (decoder fault, false standstill flag)	OQ-008	TI data
284	SG-03	F03-101 share	UNRELEASED	Failure-mode share of U6 set by sev10: No speed pulses although the wheel turns (unsupplied, output static)	OQ-008	TI data
285	SG-03	F03-102 share	UNRELEASED	Failure-mode share of U6 set by sev10: Other faults (speed too high, SPI loss) without a false standstill	OQ-008	TI data
286	SG-03	F03-103 share	JUDGMENT	Failure-mode share of WSS front end set by sev10: Open, short or clamp failure that stops the sensor pulses	OQ-007	TI data
287	SG-03	F03-104 share	JUDGMENT	Failure-mode share of WSS front end set by sev10: Faults without loss of pulses	OQ-007	TI data
288	SG-03	F03-150 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	OQ-007	TI data
289	SG-03	F03-151 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Transceiver stays awake when nSTB_CAN goes low (INH held high)	OQ-007	TI data
290	SG-04	F04-001 share	JUDGMENT	Failure-mode share of U7 set by sev10: Faults that add force or remove a protection unrelated to release: output stage drives the apply direction without a command (F03-001, 0.04), thermal protection lost (F03-013, 0.05), OUTx short on the terminal driven only for release (half of F03-012, 0.025)	OQ-007	TI data
291	SG-04	F04-002 share	JUDGMENT	Failure-mode share of U7 set by sev10: Output stage drives the release direction without a command (diagonal FET pair shorted or gate drive stuck on)	OQ-007	TI data
292	SG-04	F04-003 share	JUDGMENT	Failure-mode share of U7 set by sev10: Input logic fault (EN/IN1 or PH/IN2 buffer, state machine) drives the bridge in the release direction without a command	OQ-007	TI data
293	SG-04	F04-014 share	JUDGMENT	Failure-mode share of U7 set by sev10: Input logic fault inverts the direction: a commanded apply drives the release end stop and ends on a stall	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
294	SG-04	F04-004 share	JUDGMENT	Failure-mode share of U7 set by sev10: DRVOFF no longer disables the bridge	OQ-007	TI data
295	SG-04	F04-005 share	JUDGMENT	Failure-mode share of U7 set by sev10: Current-sense output (IPROPI) reads low or zero	OQ-007	TI data
296	SG-04	F04-015 share	JUDGMENT	Failure-mode share of U7 set by sev10: Current-sense output (IPROPI) reads high (gain or offset error)	OQ-007	TI data
297	SG-04	F04-006 share	JUDGMENT	Failure-mode share of U7 set by sev10: Register corruption unlocks SPI control and drives the release, or lowers OCP_SEL/S_ITRIP so the apply stops below holding force	OQ-007	TI data
298	SG-04	F04-007 share	JUDGMENT	Failure-mode share of U7 set by sev10: Fault reporting (nFAULT, STATUS, SPI readback) lost or wrong	OQ-007	TI data
299	SG-04	F04-008 share	JUDGMENT	Failure-mode share of U7 set by sev10: Outputs off or high impedance; the bridge cannot drive	OQ-007	TI data
300	SG-04	F04-009 share	JUDGMENT	Failure-mode share of U7 set by sev10: VM or GND pin short, internal supply short	OQ-007	TI data
301	SG-04	F04-012 share	JUDGMENT	Failure-mode share of U7 set by sev10: OUTA or OUTB shorted to VM or GND on the terminal the apply must drive	OQ-007	TI data
302	SG-04	F04-010 share	JUDGMENT	Failure-mode share of U7 set by sev10: Over-current protection lost	OQ-007	TI data
303	SG-04	F04-011 share	JUDGMENT	Failure-mode share of U7 set by sev10: Other internal faults (charge pump, oscillator, SPI timing, POR on defaults) that stop the bridge	OQ-007	TI data
304	SG-04	F04-020 share	JUDGMENT	Failure-mode share of U14 set by sev10: CPU, memory or bus fault produces an erroneous EPB release command	OQ-007	TI data
305	SG-04	F04-021 share	JUDGMENT	Failure-mode share of U14 set by sev10: EPB control pins (U14.2 DRVOFF, U14.11, U14.98) stuck in the release-drive state (port fault the lockstep does not see)	OQ-007	TI data
306	SG-04	F04-027 share	JUDGMENT	Failure-mode share of U14 set by sev10: PH/IN2 drive pin (U14.98) stuck at the release level	OQ-007	TI data
307	SG-04	F04-028 share	JUDGMENT	Failure-mode share of U14 set by sev10: EPB control pins stuck in the off state (DRVOFF high or EN/IN1 low)	OQ-007	TI data
308	SG-04	F04-022 share	JUDGMENT	Failure-mode share of U14 set by sev10: SPI-D peripheral fault writes wrong data to U7	OQ-007	TI data
309	SG-04	F04-023 share	JUDGMENT	Failure-mode share of U14 set by sev10: Lockstep comparator, ECC or error-signal module fault	OQ-007	TI data
310	SG-04	F04-024 share	JUDGMENT	Failure-mode share of U14 set by sev10: Isense_EPB ADC channel reads low or zero	OQ-007	TI data
311	SG-04	F04-029 share	JUDGMENT	Failure-mode share of U14 set by sev10: Isense_EPB ADC channel reads high	OQ-007	TI data
312	SG-04	F04-026 share	JUDGMENT	Failure-mode share of U14 set by sev10: CAN receive path (MCAN, message RAM) delivers a false EPB release or drive-away request	OQ-007	TI data
313	SG-04	F04-025 share	JUDGMENT	Failure-mode share of U14 set by sev10: Other MCU functions (BLDC control, other peripherals)	OQ-007	TI data
314	SG-04	F04-030 share	JUDGMENT	Failure-mode share of U3 set by sev10: Watchdog or error monitor fails to act, or NRST cannot reset the MCU	OQ-007	TI data
315	SG-04	F04-034 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 (3.3 V, MCU I/O and U7 logic) regulates high	OQ-007	TI data
316	SG-04	F04-035 share	JUDGMENT	Failure-mode share of U3 set by sev10: Rail monitors (EXT_VMON1 on the 1.25 V core, LDO overvoltage) stuck at 'good'	OQ-007	TI data
317	SG-04	F04-032 share	JUDGMENT	Failure-mode share of U3 set by sev10: Spurious reset or safe state	OQ-007	TI data
318	SG-04	F04-033 share	JUDGMENT	Failure-mode share of U3 set by sev10: Other PMIC functions (regulators low or lost, pedal supplies, other monitors, SAFE_OUT1 failing to assert)	OQ-007	TI data
319	SG-04	F04-040 share	JUDGMENT	Failure-mode share of U5 set by sev10: CUTOFF1 output stuck on	OQ-007	TI data
320	SG-04	F04-041 share	JUDGMENT	Failure-mode share of U5 set by sev10: CUTOFF1 output stuck off	OQ-007	TI data
321	SG-04	F04-042 share	JUDGMENT	Failure-mode share of U5 set by sev10: Other gate-driver functions (BLDC bridge)	OQ-007	TI data
322	SG-04	F04-110 share	JUDGMENT	Failure-mode share of U4 set by sev10: 1.25 V core regulated high (half of TI's 'output out of specification' mode)	OQ-007	TI data
323	SG-04	F04-111 share	JUDGMENT	Failure-mode share of U4 set by sev10: High-side FET stuck on: core pulled toward VCC_6V0 (half of TI's 'HS or LS FET stuck on' mode)	OQ-007	TI data
324	SG-04	F04-120 share	JUDGMENT	Failure-mode share of U2 set by sev10: High-side FET short: 12 V rail pulled toward 48V/12V_P	OQ-007	TI data
325	SG-04	F04-121 share	JUDGMENT	Failure-mode share of U2 set by sev10: Output low or lost, regulation faults within the PMIC input range	OQ-007	TI data
326	SG-04	F04-150 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Receiver or transmitter fail, stuck in sleep, bus dominant, erroneous fault report	OQ-007	TI data
327	SG-04	F04-151 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Transceiver stays awake when nSTB_CAN goes low (INH held high)	OQ-007	TI data
328	SG-04	F04-155 share	JUDGMENT	Failure-mode share of U14 set by sev10: CAN transmit path (MCAN, message RAM) corrupts the EPB status (hold or availability reported wrongly)	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
329	SG-05	F05-001 share	UNRELEASED	Failure-mode share of U6 set by sev10: Decoded speed wrong or erratic while pulses continue (current-threshold drift, decoder logic or internal timing reference fault, V1P5 glitches)	OQ-008	TI data
330	SG-05	F05-002 share	UNRELEASED	Failure-mode share of U6 set by sev10: No speed pulses although the wheel turns (current comparator, decoder, oscillator or WSSO driver fault; VCC5 or VIO pin open)	OQ-008	TI data
331	SG-05	F05-003 share	UNRELEASED	Failure-mode share of U6 set by sev10: Configuration register or SPI interface fault changes the decoding mode or thresholds; silent reset to defaults	OQ-008	TI data
332	SG-05	F05-004 share	UNRELEASED	Failure-mode share of U6 set by sev10: SDO output stuck or readback data wrong	OQ-008	TI data
333	SG-05	F05-005 share	UNRELEASED	Failure-mode share of U6 set by sev10: Internal short from VBAT (12 V) to VIO or VCC5	OQ-008	TI data
334	SG-05	F05-006 share	UNRELEASED	Failure-mode share of U6 set by sev10: Sensor-supply protection or open/short diagnostics lost, spurious fault flags, other faults that leave the speed correct	OQ-008	TI data
335	SG-05	F05-050 share	JUDGMENT	Failure-mode share of U7 set by sev10: SPI pin fault (SDO driven outside its select window, SDI or SCLK loaded) corrupts WSS001 frames on the shared SPI-D	OQ-007	TI data
336	SG-05	F05-051 share	JUDGMENT	Failure-mode share of U7 set by sev10: Other U7 functions	OQ-007	TI data
337	SG-05	F05-060 share	JUDGMENT	Failure-mode share of U14 set by sev10: CPU, memory or bus fault in the speed computation, the validity flag or the frame content	OQ-007	TI data
338	SG-05	F05-061 share	JUDGMENT	Failure-mode share of U14 set by sev10: eCAP, Input X-BAR or AIO203 input path fault: captures missed, doubled or mis-timed	OQ-007	TI data
339	SG-05	F05-062 share	JUDGMENT	Failure-mode share of U14 set by sev10: PLL or clock-divider fault: SYSCLK wrong	OQ-007	TI data
340	SG-05	F05-063 share	JUDGMENT	Failure-mode share of U14 set by sev10: MCAN module or message-RAM fault: wheel-speed frames lost, frozen or corrupted	OQ-007	TI data
341	SG-05	F05-064 share	JUDGMENT	Failure-mode share of U14 set by sev10: Lockstep comparator, ECC or error-signal module fault	OQ-007	TI data
342	SG-05	F05-065 share	JUDGMENT	Failure-mode share of U14 set by sev10: Missing-clock detection or DCC fault, or their configuration lost	OQ-007	TI data
343	SG-05	F05-066 share	JUDGMENT	Failure-mode share of U14 set by sev10: Other MCU functions (BLDC and EPB control, other peripherals)	OQ-007	TI data
344	SG-05	F05-080 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO2 (5 V) regulates high or its pass element shorts toward VCC_6V0	OQ-007	TI data
345	SG-05	F05-081 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO2 (5 V) low or drifting, below the U6 minimum while the CAN transceivers still work	OQ-007	TI data
346	SG-05	F05-082 share	JUDGMENT	Failure-mode share of U3 set by sev10: LDO1 (3.3 V) regulates high	OQ-007	TI data
347	SG-05	F05-083 share	JUDGMENT	Failure-mode share of U3 set by sev10: Rail monitors (LDO1, LDO2 overvoltage), watchdog, error monitor or NRST fail to act	OQ-007	TI data
348	SG-05	F05-084 share	JUDGMENT	Failure-mode share of U3 set by sev10: Other PMIC functions (other regulators, rail loss, pedal supplies)	OQ-007	TI data
349	SG-05	F05-093 share	JUDGMENT	Failure-mode share of U2 set by sev10: 12 V output low, in a band where U3 and U14 run but U6 VBAT is below its minimum	OQ-007	TI data
350	SG-05	F05-094 share	JUDGMENT	Failure-mode share of U2 set by sev10: Other U2 faults (output lost, 12 V overvoltage)	OQ-007	TI data
351	SG-07	F07-001 share	JUDGMENT	Failure-mode share of C8 set by sev10: Internal short, hard (half of the 20 % short mode)	OQ-007	TI data
352	SG-07	F07-002 share	JUDGMENT	Failure-mode share of C8 set by sev10: Internal short, resistive (half of the 20 % short mode)	OQ-007	TI data
353	SG-07	F07-003 share	JUDGMENT	Failure-mode share of C8 set by sev10: Venting after internal heating (ESR rise with ripple)	OQ-007	TI data
354	SG-07	F07-004 share	JUDGMENT	Failure-mode share of C8 set by sev10: Open, capacitance loss or ESR rise without venting	OQ-007	TI data
355	SG-07	F07-005 share	JUDGMENT	Failure-mode share of C7, C9, C10 set by sev10: Short, hard	OQ-007	TI data
356	SG-07	F07-006 share	JUDGMENT	Failure-mode share of C7, C9, C10 set by sev10: Short, resistive	OQ-007	TI data
357	SG-07	F07-011 share	JUDGMENT	Failure-mode share of J3, J4 set by sev10: Joint degrades to high resistance and heats (half of the 70 % open mode)	OQ-007	TI data
358	SG-07	F07-012 share	JUDGMENT	Failure-mode share of J3, J4 set by sev10: Clean open (crack, lift)	OQ-007	TI data
359	SG-07	F07-013 share	JUDGMENT	Failure-mode share of J3, J4 set by sev10: Short between J3 and J4 or to the harness	OQ-007	TI data
360	SG-07	F07-028 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 drain-source short (40 % of Q1)	OQ-007	TI data
361	SG-07	F07-029 share	JUDGMENT	Failure-mode share of Q1, Q2 set by sev10: Q1 other modes; any Q2 mode	OQ-007	TI data
362	SG-07	F07-030 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Transceiver stays awake when nSTB_CAN goes low (INH held high)	OQ-007	TI data
363	SG-07	F07-031 share	JUDGMENT	Failure-mode share of U8, U10 set by sev10: Other transceiver faults	OQ-007	TI data
364	SG-07	F07-032 share	JUDGMENT	Failure-mode share of INH network set by sev10: R156 open: INH_CAN floats instead of going low	OQ-007	TI data
365	SG-07	F07-033 share	JUDGMENT	Failure-mode share of INH network set by sev10: Other faults	OQ-007	TI data

#	Where	Item	Reason code	Basis	Closes with	Closes when we have
366	SG-07	F07-040 share	JUDGMENT	Failure-mode share of C5, C6, C21, C22, C61, C75, C76, C23, C24, C68 set by sev10: Crack or dielectric short, hard	OQ-007	TI data
367	SG-07	F07-041 share	JUDGMENT	Failure-mode share of C5, C6, C21, C22, C61, C75, C76, C23, C24, C68 set by sev10: Crack short, resistive (about 3-300 Ohm)	OQ-007	TI data
368	SG-07	F07-043 share	JUDGMENT	Failure-mode share of C5, C6, C21, C22, C61, C75, C76, C23, C24, C68 set by sev10: Crack or dielectric short, hard	OQ-007	TI data
369	SG-07	F07-044 share	JUDGMENT	Failure-mode share of C5, C6, C21, C22, C61, C75, C76, C23, C24, C68 set by sev10: Crack short, resistive (about 3-300 Ohm)	OQ-007	TI data
370	SG-07	F07-046 share	JUDGMENT	Failure-mode share of C28, C60, C73, C74 set by sev10: Internal short, hard (half of the 20 % short mode)	OQ-007	TI data
371	SG-07	F07-047 share	JUDGMENT	Failure-mode share of C28, C60, C73, C74 set by sev10: Internal short, resistive	OQ-007	TI data
372	SG-07	F07-048 share	JUDGMENT	Failure-mode share of C28, C60, C73, C74 set by sev10: Venting after internal heating (ESR rise with ripple)	OQ-007	TI data
373	SG-07	F07-049 share	JUDGMENT	Failure-mode share of C28, C60, C73, C74 set by sev10: Open, capacitance loss or ESR rise without venting	OQ-007	TI data
374	SG-07	F07-050 share	JUDGMENT	Failure-mode share of C96, C97 set by sev10: Crack or dielectric short, hard	OQ-007	TI data
375	SG-07	F07-051 share	JUDGMENT	Failure-mode share of C96, C97 set by sev10: Crack short, resistive (EPB-201: 2-20 A)	OQ-007	TI data
376	SG-07	F07-053 share	JUDGMENT	Failure-mode share of C96, C97 set by sev10: Crack or dielectric short, hard	OQ-007	TI data
377	SG-07	F07-054 share	JUDGMENT	Failure-mode share of C96, C97 set by sev10: Crack short, resistive	OQ-007	TI data
378	SG-07	F07-056 share	JUDGMENT	Failure-mode share of U7 set by sev10: VM-to-GND internal short, hard (half of F03-009)	OQ-007	TI data
379	SG-07	F07-057 share	JUDGMENT	Failure-mode share of U7 set by sev10: VM-to-GND internal short, resistive	OQ-007	TI data
380	SG-07	F07-058 share	JUDGMENT	Failure-mode share of U7 set by sev10: Other U7 faults (output stage, logic, OCP and thermal shutdown lost)	OQ-007	TI data
381	SG-07	F07-060 share	JUDGMENT	Failure-mode share of U2 set by sev10: VIN-to-PGND internal short, hard	OQ-007	TI data
382	SG-07	F07-061 share	JUDGMENT	Failure-mode share of U2 set by sev10: VIN-to-PGND internal short, resistive	OQ-007	TI data
383	SG-07	F07-062 share	JUDGMENT	Failure-mode share of U2 set by sev10: High-side FET short: 12 V rail pulled toward 48V/12V_P	OQ-007	TI data
384	SG-07	F07-063 share	JUDGMENT	Failure-mode share of U2 set by sev10: Cycle-by-cycle current limit or hiccup lost	OQ-007	TI data
385	SG-07	F07-064 share	JUDGMENT	Failure-mode share of U2 set by sev10: Output low or lost, other regulation faults	OQ-007	TI data
386	SG-07	F07-065 share	JUDGMENT	Failure-mode share of R33, R35 set by sev10: R33 open or R35 short: U2 drives 12 V toward the input	OQ-007	TI data
387	SG-07	F07-066 share	JUDGMENT	Failure-mode share of R33, R35 set by sev10: R33 short, R35 open, drift within tolerance	OQ-007	TI data
388	SG-07	F07-070 share	JUDGMENT	Failure-mode share of C25, C26, C27, C31-C36, C89, C62 set by sev10: Short, hard (below the U2 hiccup entry)	OQ-007	TI data
389	SG-07	F07-071 share	JUDGMENT	Failure-mode share of C25, C26, C27, C31-C36, C89, C62 set by sev10: Crack or wear-out short, resistive (about 1-15 Ohm)	OQ-007	TI data
390	SG-07	F07-073 share	JUDGMENT	Failure-mode share of C25, C26, C27, C31-C36, C89, C62 set by sev10: Short, hard	OQ-007	TI data
391	SG-07	F07-074 share	JUDGMENT	Failure-mode share of C25, C26, C27, C31-C36, C89, C62 set by sev10: Short, resistive	OQ-007	TI data
392	SG-07	F07-082 share	JUDGMENT	Failure-mode share of J7, J8, J9 set by sev10: Joint degrades to high resistance and heats (half of the 70 % open mode)	OQ-007	TI data
393	SG-07	F07-083 share	JUDGMENT	Failure-mode share of J7, J8, J9 set by sev10: Clean open (crack, lift)	OQ-007	TI data

sev10 Open questions

Subject: Corner brake ECU, TI TIDA-020106 PCB VerB · FMEDA ID: S10-QLN-FMEDA-001 · Rev A (draft for client review) · Customer: Quillon Motors

Questions from the running log S10-QLN-OQL-001 that this FMEDA relies on.

ID	Raised	FMEDA use	Question	Assumption used until answered	Owner	Status	Answer
OQ-002	2026-09-27	SG-01, SG-02, SG-03, SG-04, SG-05, Safety mechanisms	U3 is ordered as O386005QDCARQ1, a TPS653860-Q1 orderable listed as Active / Production in the datasheet's package addendum (SLVSFQ1A). TI uses `O3860xx` part numbers for NVM-configured variants (TI E2E thread 1611363). Which NVM configuration does O386005 carry (monitor thresholds, watchdog mode and timing, reset and SAFE_OUT behaviour)?	TPS653860-Q1 configured as described in TIDUFI0 §2.4.1.2. Thresholds marked `ASSUMED`.	Client (via TI)	Open	
OQ-004	2026-09-27	SG-07	J1–J9 and J11–J20 are single-pin wire solder pads with no part fitted (BOM item 33, `Pin_*` footprints). They include battery input (J3/J4, 12 A) and motor phases (J7–J9, 16 A RMS). J10 (UART and BOOT1) and J21–J23 (angle sensor SIN/COS) are 2.54 mm pin headers. What is the production harness and connector concept?	Production uses a sealed automotive connector system rated for the phase and battery currents. Harness-interface ratings marked `ASSUMED`.	Client	Open	
OQ-007	2026-09-27	FIT data, IC failure-mode shares, SG-01, SG-02, SG-07, Safety mechanisms	The following safety documents are available only on request or under NDA: TPS653860-Q1 safety manual/FMEDA; DRV3263-Q1 safety manual (SFFSBB3, marked "TI Confidential – NDA"; sev10 has not used it); DRV8263-Q1 FS package ("DRV8263-Q1-FS"); TMAG6180-Q1 FS package ("TMAG618X-Q1-FS"); LM68645-Q1 FMEDA; F29P32x safety manual. In addition, the public datasheets for TPS653860-Q1 (SLVSFQ1A, 14 pp) and DRV3263-Q1 (SLVSLU5, 13 pp) are abbreviated; the full datasheets, with electrical characteristics and diagnostic descriptions, are on request. Can the client obtain them under its NDA with TI?	Generic failure-rate data (SN 29500 / IEC 61709 basis) plus datasheet-documented diagnostics. All such values marked `ASSUMED`.	Client (via TI)	Open	
OQ-008	2026-09-27	FIT data, Goals, targets, SG-05, Safety mechanisms	WSS001 (U6, wheel-speed decoder) and ESD2CAN48-Q1 (U9, U11, CAN ESD protection) have no public product page or datasheet on ti.com. What is their release status, and can datasheets be provided? For the FMEDA: the WSS001 register map, reset flag and frame integrity (CRC or fixed bits), the VBAT and VCC5 limits, and the split of the wrong-speed failure mode into gross and small errors.	Function per TIDUFI0 §2.3.3 and the schematic only. Ratings marked `ASSUMED`.	Client (via TI)	Open	
OQ-009	2026-09-27	Safety mechanisms	Pedal force (PFS, J12) and pedal travel (PTS, J14) come in through wire pads as analog or SENT signals (TIDUFI0: "Analog/SENT"; the input circuit has a 10 kΩ pull-up and a 69.8 kΩ/100 kΩ divider). Each signal is routed to two MCU pins (R128/R145, R129/R144). The sensors are powered from 5Vp1/5Vp2 (J15/J11). Which signal type, which sensors (TI shows TMAG3101-Q1 + LDC5072-Q1 for travel; force sensor unspecified), and what plausibility checks does the application use?	SENT, two independent sensors, sensors themselves out of scope; supply and input path in scope.	Client	Open	
OQ-010	2026-09-27	FIT data, Goals, targets, SG-07	What mission profile applies: temperature at the ECU mounting location, operating hours, lifetime? TI specifies the reference design for −25 to 75 °C open-frame lab use only, which is not an automotive profile.	−40 to +105 °C board ambient, 15 years, 8,000 operating hours. Marked `ASSUMED`. Supply variant: see OQ-011.	Client	Open	

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OQ-014	2026-09-27	SG-03, Safety mechanisms	TIDUFI0 §2.4.1.1 and SDAA375 describe an overvoltage cut-off in which the F29 CMPSS acts through the TCAN1043H EN/INH pins to shut down the supply chain. TI classifies TCAN1043H-Q1 as Functional Safety-Capable, not developed to an ASIL. What ASIL decomposition and fault-tolerant time interval apply? And since the CMPSS must be configured by firmware, which is available only through TI sales, how is the mechanism verified?	Mechanism credited as a detection control at reduced effectiveness until the decomposition is confirmed. Marked `ASSUMED`.	Client (via TI)	Open	
OQ-016	2026-09-27	FIT data	The IPC-356 header lists a six-layer stackup (Top, GND, Power, Sig4, GND, Bottom), but the Gerber package contains outer copper layers only (GTL/GBL). What is the production stackup, copper weight and PCB material?	Six-layer FR-4, high-Tg; PCB-level ratings marked `ASSUMED`.	Client	Open	
OQ-017	2026-09-27	SG-07	The 48 V variant is specified for 32–60 V, and the LM74930-Q1 overvoltage trip is set at 60.6 V. Which 48 V supply standard (ISO 21780 / LV 148) and which transient and load-dump profiles apply?	ISO 21780 applies. Protection margins are evaluated against it.	Client	Open	
OQ-018	2026-09-27	FIT data, SG-07	26 BOM lines don't state an AEC-Q grade. For several, the part-number series suggests general-purpose rather than automotive parts: Murata GRM (items 4, 10, 14, 16, 21), TDK C1608 (item 17) and KEMET C0402C…RAC (item 13; KEMET's link resolves to its commercial X7R series datasheet). sev10 will confirm each against the manufacturer datasheet during the datasheet step. Are the confirmed commercial-grade parts replaced by AEC-Q200 equivalents in production?	Production uses AEC-Q200 equivalents with the same value and rating. Recorded as a design finding for the published BOM.	Client	Open	
OQ-021	2026-09-27	FTTI, Safety mechanisms	What fault-tolerant time intervals apply to each safety goal, and how fast must the corner follow a change in friction share when regeneration drops out? For the FMEDA: how the SG-05 FTTI divides between detection in this ECU, CAN transport and the brake controller's reaction.	SG-01 100 ms, SG-02 200 ms, SG-03 300 ms, SG-04 1 s, SG-05 50 ms. `ASSUMED`.	Client	Open	
OQ-022	2026-09-27	SG-02, Safety mechanisms	Is a fail-silent corner (brake released, fault reported, other corners and yaw control compensate) acceptable at vehicle level?	Yes. `ASSUMED`.	Client	Open	
OQ-023	2026-09-27	SG-01, SG-04, Safety mechanisms	Does the service brake release when the caliper motor is unpowered, and does the EPB spindle hold without power?	Service brake releases; EPB self-locks. `ASSUMED`.	Client	Open	
OQ-025	2026-09-27	SG-07, Safety mechanisms	How are the four corner ECUs split across power supplies and CAN buses?	Two independent domains (e.g. diagonal). `ASSUMED`.	Client	Open	
OQ-028	2026-09-27	Safety mechanisms	Which design verification will the module receive before release (bench functional tests, fault injection, worst-case circuit analysis, environmental and EMC testing per ISO 16750 / ISO 21780 / CISPR 25, HIL)? TI's published test results for TIDA-020106 cover the PMIC power-on sequence and MCU reset only.	Current detection controls are TI's published validation plus generic functional bench testing of the reference design. D = 9 for causes normal operation would reveal, D = 10 for causes only visible under fault, stress or temperature extremes. Proposed verification is recorded as DFMEA detection actions.	Client	Open	

ID	Raised	FMEDA use	Question	Assumption used until answered	Owner	Status	Answer
OQ-029	2026-09-27	Safety mechanisms	The published BOM fits R57, R58 and Q6 together with the DRV3263A (U5). The schematic labels U5 pin 31 "PVDD for DRV3233", so R58 is the DRV3233 supply strap; with the DRV3263 fitted it ties CUTOFF1 (pin 31), and through R57 the gate of the EPB cut-off FET Q11, to 48V/12V_P. Q6 is the alternative VCP-based gate drive for the DRV3233. Which of R57, R58, Q6, R53 and C63 are fitted in the production configuration, and which device drives Q11?	Analysed as published (all fitted) and recorded as a design finding; the production intent is assumed to be R58 not fitted.	Client (via TI)	Open	
OQ-030	2026-09-27	SG-07	Is the board conformally coated in production? The design rules in the Gerber package set 7.87 mil (0.2 mm) general clearance and 15.75 mil (0.4 mm) for the 48 V to GND rule; several 48 V pads sit 0.4–0.6 mm from other nets (for example C96 to R91, which is on 3.3 V).	Uncoated (worst case); spacing below 0.6 mm between 48 V and other nets recorded as a design finding.	Client	Open	
OQ-032	2026-09-27	Goals, targets, SG-01, SG-03, Safety mechanisms	How does the firmware configure and supervise U7? Specifically: idle state of DRVOFF_EPB and IN1/IN2, S_MODE, OCP_SEL, S_ITRIP, fault reaction (latch or retry), SPI_IN and register lock, DRV_SEL, periodic readback, reaction to a persistent nFAULT, stall-termination threshold, minimum run time and timeout. Are there software safety requirements for the EPB?	Worst credible configuration (defaults, retry, SPI_IN unlocked on corruption). Proposed software requirements are recorded as DFMEA actions.	Client	Open	
OQ-034	2026-09-28	SG-01	What are the caliper BLDC motor pole-pair count and maximum speed, the angle magnet grade, size, holder and the board side it faces, the air gap to U12 (top) and U13 (bottom) over temperature and life, and centring tolerance?	Pole pairs odd, max electrical frequency 1000 Hz (TIDUFI0 Table 1-1), field adequate at both sensors: ASSUMED.	Client	Open	
OQ-035	2026-09-28	Safety mechanisms	Tone-wheel tooth count, tyre rolling circumference, the SG-03 standstill speed threshold and confirmation time, and the wheel-speed sensor type (2-level, AK, HR-AK) with its reverse-polarity behaviour.	48 teeth, 2.0 m circumference, 2-level active sensor: ASSUMED.	Client	Open	
OQ-038	2026-09-28	SG-01, Safety mechanisms	Which plausibility checks does the firmware apply to the angle channels (channel compare, sin^2+cos^2, quadrant consistency, range), wheel speed (standstill confirmation) and pedal inputs (dual-sensor compare)? Which ADC modules and triggers are used for each channel? Also: which angle channel the firmware uses for commutation, and whether the other channel is used only for comparison or fused into the angle (the SG-01 FMEDA treats U13 as the monitor channel).	Not credited until specified; proposed requirements recorded as DFMEA actions.	Client	Open	
OQ-039	2026-09-28	SG-02, SG-05	Do both CAN buses carry the clamp-force requests and status to every corner, or does each corner get its requests on one bus only? What are the arbitration and data bit rates, sample points, transmitter delay compensation, node count, cable lengths, and which nodes terminate each bus? For the FMEDA: which CAN channel or channels carry the wheel speed, and the CAN bit-timing tolerance.	Requests on both buses; 500 kbit/s / 2 Mbit/s; this ECU is not a bus end node: ASSUMED.	Client	Open	
OQ-040	2026-09-28	SG-02, SG-05, Safety mechanisms	How is each corner ECU's position (and the CAN data IDs that follow from it) set in production: coding pins, end-of-line coding or software variant? Which E2E profile (CRC, alive counter, data ID, timeout) protects the brake request and status frames, and what reaction is required on timeout?	E2E with a per-corner data ID and a request timeout will be specified; not credited until then.	Client	Open	

ID	Raised	FMEDA use	Question	Assumption used until answered	Owner	Status	Answer
OQ-041	2026-09-28	SG-01, Safety mechanisms	After the SDAA375 CMPSS trip drops INH_CAN, how is the off state held? Normal bus traffic is a valid wake-up pattern and restores INH within milliseconds; EN or WAKERQ state can also block the sleep. Must firmware stop both motors before any intentional INH drop, and is a hardware latch or a clamp/chopper on 48V/12V_P acceptable?	Not credited as a latched safe state; a hardware latch is proposed as a design action.	Client (via TI)	Open	
OQ-043	2026-09-28	Safety mechanisms	What clamp-force accuracy and overshoot tolerance per corner does the vehicle require, i.e. at what force error does a deviation become a safety effect (wrong force, SG-01/SG-02) rather than a quality deviation? Is clamp force estimated from motor current and angle (no force sensor)?	Force estimated from motor current (no force sensor, OQ-020); an error above about 10 % of request is treated as FE-03: ASSUMED.	Client	Open	
OQ-044	2026-09-28	Goals, targets, SG-07, Safety mechanisms	Several board faults (a resistive crack short of a 48 V bus capacitor below the U1 trip level, CAF on 48 V nets, an overheated wire pad) can char the laminate and cause smoke or fire at the wheel corner. The HARA has no hazardous event or safety goal for a thermal event of the ECU. Should one be added at vehicle level, and with what ASIL?	HARA Rev B (2026-09-28) adds HE-20 and SG-07 "Avoid a thermal event (smoke, fire) of the corner ECU" at ASIL B (S3, E4, C1; A-12). The DFMEA rates the board-level thermal chains at the new effect FE-29 (PCB-202, PCB-303); per-part crack rows keep their braking effect and point to PCB-202. Please confirm the ASIL and state the FTTI (time from a resistive fault to ignition), which is ASSUMED in the HARA.	Client	Open	
OQ-046	2026-09-28	PMHF target, SG-02, SG-03, SG-07	ISO 26262-5 sets the PMHF target per safety goal for the whole item (for ASIL D below 10 FIT). What share of each goal's budget is allocated to one corner brake ECU, given four corners and the central brake controller?	Compared with the item-level target; the margin is stated, not a pass.	Client	Open	
OQ-047	2026-09-28	SG-03, Safety mechanisms	When the EPB is applied without a request while the vehicle moves, how much rear clamp force can build before vehicle stability is affected at speed, and how fast does the EPB actuator build force (force against time from the start of motion)? The SG-03 stops open the supply cut-off (Q11) or put U7 to sleep: they end the apply but do not release the force already built.	The stop acts within the provisional 300 ms FTTI and the force built in that time is not hazardous. Credit marked `ASSUMED` (PROVISIONAL); the Summary shows the SPFM without it.	Client	Open	
OQ-048	2026-09-28	Goals, targets, SG-01	How fast does the service caliper release when the motor is de-energised, and how much does a shorted inverter phase or a shorted winding (motor braked by back-EMF) slow that release? Please give clamp force against time after de-energising, from full force, with the phases open and with one phase shorted, together with the motor's back-EMF constant and winding resistance.	Unpowered release meets the provisional 100 ms FTTI with the phases open, and misses it with a phase shorted. Marked `ASSUMED`.	Client	Open	
OQ-049	2026-09-28	Goals, targets, Safety mechanisms	Which checks does the brake controller apply to each corner's wheel speed: cross-wheel deviation threshold and confirmation time, wheel-acceleration limit, loss-of-pulse timeout, E2E timeout, and handling of a sensor fault during an ABS or ESC intervention? What wheel-speed error at one wheel does ABS/ESC tolerate without a hazard?	Threshold max(2 km/h, 5 %) for 20 ms; loss-of-pulse timeout of two expected periods; E2E timeout 30 ms; 1 % error tolerated. Marked `ASSUMED`.	Client	Open	

ID	Raised	FMEDA use	Question	Assumption used until answered	Owner	Status	Answer
OQ-050	2026-09-28	Goals, targets	What status does each corner ECU send to the brake controller (content, cycle, E2E profile, on which CAN channels), what timeout and reaction does the brake controller apply when the status stops, freezes or reports "unavailable/limited", and how long may a corner take from an unplanned reset to reporting again? Is the corner required to hold "unavailable" after a reset whose cause it did not command until its start-up tests pass?	Status frame every 10 ms on both channels with CRC and alive counter; brake-controller timeout of 3 frames and redistribution within the 200 ms provisional FTTI; after an unplanned reset U14 reports "unavailable" until its start-up tests pass (PMC-419). ASSUMED.	Client	Open	
OQ-052	2026-09-28	Goals, targets, SG-04, Safety mechanisms	Can one rear EPB alone hold the vehicle at GVWR, with a trailer if towing is permitted, on the steepest parking gradient, (a) at its normal clamp force and (b) after a re-clamp? How fast does the other rear corner re-clamp after a CAN report that this corner lost its hold? How much clamp force does the EPB lose in the first 50, 100 and 300 ms of an unintended release?	One rear corner holds the vehicle after a re-clamp; the re-clamp completes within the 1 s FTTI; a Q11 stop within 100 ms keeps most of the force. ASSUMED.	Client	Open	
OQ-053	2026-09-28	Goals, targets, SG-04	When the corner detects a fault and standstill cannot be confirmed (wheel speed invalid, CAN speed missing), which reaction applies to the EPB: release and inhibit (SG-03) or hold (SG-04)? Does losing the standstill confirmation during auto-hold ever release the hold? If the standstill hold is first taken by the service brake, do the SG-01 reactions (release to zero force on a request timeout, CAN-102; release first after a PMIC reset, PMC-419) wait for the EPB to take over?	A fault reaction at unconfirmed standstill keeps the hold; only a valid E2E-protected driver or drive-away request releases it; SG-01 reactions at standstill hand over to the EPB first. ASSUMED.	Client	Open	
OQ-054	2026-09-28	Goals, targets	What share of 48 V MLCC crack shorts and aluminium-electrolytic internal shorts on this board stay in the resistive band (about 3 Ohm to a few hundred Ohm at 54 V) long enough to heat the site, rather than going straight to a hard short that trips U1? And what is the lowest sustained power at a 1210, 0805 and 0603 site on this stack-up that reaches the laminate decomposition temperature? Both can come from the fault injection that PCB-202, BLD-401 and PCB-303 already plan (1-20 Ohm across C22, C76, C96 at 54 V).	MLCC, aluminium and IC-internal supply shorts 50 % hard, 50 % resistive; CAF 100 % resistive; FET, TVS and pad shorts 100 % hard; the resistive band is taken to reach down to about 10 W.	Client	Open	
OQ-055	2026-09-28	SG-07	Is a thermal event while the vehicle is parked and unattended (key off, 48 V still present at J3/J4) in the scope of HE-20, and should the FMEDA then use calendar hours for the nets that stay biased in sleep (48V/12V_IN, 48V/12V_IN_FILTERED, NetC7_2, NetQ2_5, D1, C7-C10, C8)?	FIT per operating hour, as for the other goals; the parked case goes to the HARA and the dependent-failure analysis.	Client	Open	

Rev	Date	Description	Author
A	2026-09-28	Draft for client review: SG-01, SG-02, SG-03, SG-04, SG-05, SG-07 computed (provisional); other goals not computed in this example; 393 assumed values registered	sev10